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OFET Laboratory

Report

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Contents

1 Introduction

A field effect transistor is a three terminal device in which the current between the two terminals source and drain is controlled by the voltage which is applied to the gate terminal. Usually, the main elements used in transistors are inorganic materials such as silicon, germanium and gallium arsenide. These devices have high rigidity and are complex in processing. Thus, many methods and materials have been investigated to further improve or to provide alternatives to these devices. One of these methods is the use of organic materials to fabricate thin film field effect transistors. As a justification to why these kind of materials can be used is that they can be processed at room temperature and also provide structural flexibility, a property that inorganic materials lack [1] [8].
In addition, even roll to roll printing fabrication of organic field effect transistors (OFETs) is possible, marking the way of flexible and cheap electronics. However, like any other real world material, they are not without their drawbacks. One of the most important drawback of organic material is that they have a far inferior charge mobility compared to well established inorganic materials such as silicon and germanium. Nevertheless, these kind of materials can be still used in devices where high switching speeds are not a requirement, where flexibility is required and a large area of the device is feasible [7]. In the mentioned case, organic materials are able to provide a cheap solution for replacing inorganic materials in this field.
There are basically two types of OFETs which can be manufactured, one in which the gate is at the bottom and the other with the gate on the top [7]. In this lab, a top gate OFET design was implemented in a step by step fabrication, which will be discussed in the methods section. Beforehand, for a better view and understanding of the fabricated device, a theory section will explain different aspects of the device from the material being used to the electrical characteristics of a transistor. After the fabrication process, the OFETs were characterized electrically and their geometrical features will also be discussed in details in the analysis section of this report.

2 Theory

2.1 Electrical Characteristics of FET

A FET has three regions of operation: cut-off, lineare and saturation. The first is the cutoff region in which the FET is off and is non-conductive. In this operation region the applied voltage between gate and source is smaller than the threshold voltage of the FET and in this region, the current between the drain and source terminal will be ideally zero. However, as we will observe, in reality there is some subthreshold current. The second region in which a FET operates is the linear region. In this region the current between the drain and source will increase linearly with drain voltage. Lastly, we have the saturation region in which no matter how much the drain voltage is increased, the drain-source current has reached its maximum value and ideally will not increase anymore [9]. To summarize the mentioned regions, the Shockley first order transistor model can be used:

$$I_{DS} = \mu C_{ox} \frac{W}{L} \begin{cases} 0 & V_{GS} < V_T \\ (V_{GS} - V_T) V_{DS} - \frac{V_{DS}^2}{2} & V_{DS} < V_{Dsat} \\ \frac{1}{2} (V_{GS} - V_T)^2 & V_{DS} > V_{Dsat} \end{cases}$$

where μ is the mobility, C_{ox} is the capacitance of the oxide in the FET device, W is the width, L is the length, V_{GS} is the gate voltage, V_T is the threshold voltage and V_{DS} is the drain voltage with voltages referenced to the source [9].
On/Off current ratio is another useful electrical characteristic of a transistor defined as [9]:

$$R_{ON,OFF} = \frac{I_{D,ON}}{I_{D,OFF}}$$

2.2 Chemistry behind Organic Semiconductors

For better understanding of the organic semiconductors, we have to take a look at their molecular structure in order to understand how these organic polymers are conductive. The first and most important part when it comes to organic materials is that their backbone is made out of carbon. The main phenomenon behind conducting polymers is the occurrence of conjugated double bonds and delocalized electrons. Carbon atoms show three different types of hybridization: the first case is when quantum states of three 2p electrons are superposed with one 2s electron to form a hybrid more favorable energy levels which is known as sp^3 hybridization. When forming double or triple bonds, carbon can also form sp^2 and sp^3 hybridization. Figure 2.1 shows the three mentioned hybridizations. When bonding, these hybridized atomic orbitals

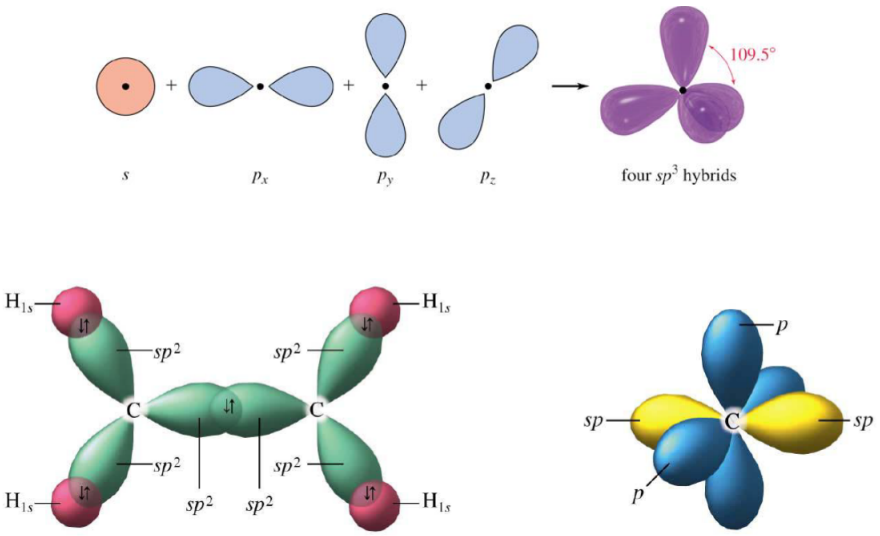


Figure 2.1: Different sp hybridizations [6]

combine to form σ bonds between sp hybrid orbitals and π bonds between p orbitals. The π bonds lead to delocalized electrons above the bonding atoms that can travel along a molecule chain if there are conjugated double bonds which in turn lead to conduction. The bonding and antibonding molecular orbitals are occupied and vacant respectively. HOMO is the highest occupied molecular orbital and LUMO is the lowest unoccupied molecular orbital. These are similar to the valence and conduction band in inorganic semiconductors in which the LUMO is the conduction band and the HOMO is the valence band. The energy gap between these two molecular orbitals is analogous to the band gap. In polymers this band gap is between 1 to 4 eV [6]. Figure 2.2 further illustrates the energy level diagram and the electron transitions in conjugated polymers: Filled polymers, ionically conducting polymers, conjugated polymers

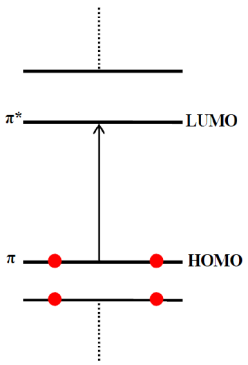


Figure 2.2: Energy diagram and electron transition in conjugated polymers [6]

and charge transport polymers all fall under the category of semiconducting polymers with charge conducting polymers being the well established semiconducting polymer in the industry [5]. In addition, semiconducting polymers can also be used to create light emitting devices

which is a very attractive and lucrative section of this technology.
The charge transport in organic semiconductors can be summarized by the following equation:

$$w_{ij} = v_o \begin{cases} exp(-2\alpha R_{ij} - \frac{E_j - E_i}{k_B T}) & E_j - E_i \geq 0 \\ exp(-2\alpha R_{ij} & E j - E_i \leq 0 \end{cases}$$

where α is the inverse localization length, R_{ij} is the distance between localized states, E_i is the energy state and v_o is the attempt-to-escape frequency[6].

2.3 Interface between the organic semiconductor and metal

One of the crucial factors that define the performance of an organic semiconductor device is the interface between the organic semiconductor and the metal. At this interface a so called Schottky barrier forms, which is caused by a Fermi energy mismatch between the metal and the semiconductor. This is dependent on the work function of the metal and the bandgap and dopant type of the semiconductor. Also, the interaction between semiconductor and metal is influenced by other factors such as covalent bonding, physisorption and chemisorption between the two materials [4] [2].

2.4 Organic Thin Film Transistors and Characteristics

A very important aspect of OFETs is the structure of the device. A top gate OFET can be seen in figure 2.3. A drain and source electrode is evaporated on a substrate, and a dielectric separates the semiconductor from the gate electrode.

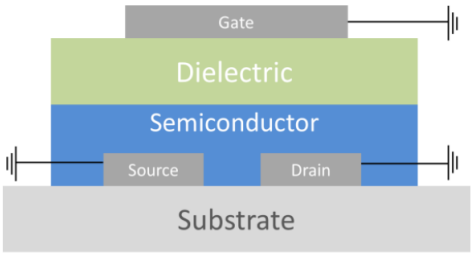


Figure 2.3: OFET structure and architecture [6]

Some other important characteristics to consider when it comes to OFETs are firstly the different operating regimes that we have in a semiconductor which can be easily identified from a drain current vs. drain voltage plot. Secondly, the On/Off ratio of drain current is important to quantify how well the device performs. Also, the current vs. voltage plot of a field effect transistor is very dependent on the geometry of the fabricated device and the materials used and other parameters such as the mobility of the device can be calculated from the measurements made in the current vs. voltage plot. It can be calculated by the formulas described in section

2.1. The threshold voltage, which is defined by the intersections with the x-axis and a linear fit to the linear region of the transistor in the transfer characteristic. From the output characteristic and the threshold current the distinction between linear and saturated region can be calculated by $V_{Dsat} = V_{GS} - V_T$. Then a parabola can be fit to the calculated points of the parabola to get the distinction in operating regimes. In figure 2.4 such a parabola is depicted in the left plot along with the IV curve characteristics of the off and on region for a P-type OFET [6].

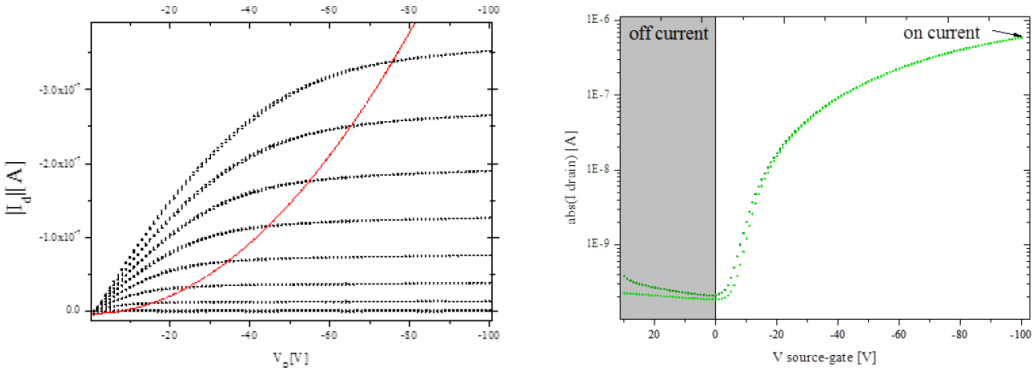


Figure 2.4: Output curve of P-type OFET (left), Transfer curve of P-type OFET (right) [6].

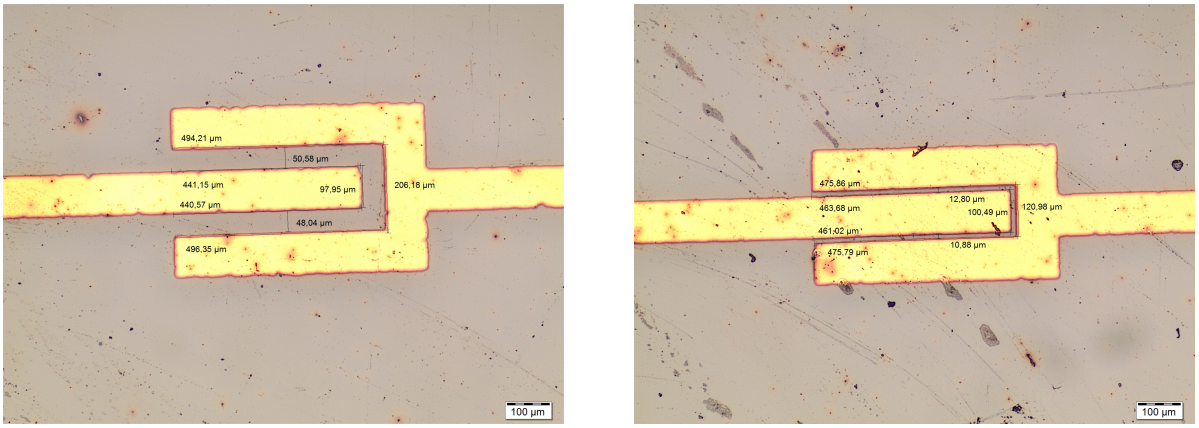
3 Methods

The fabrication of the OFET is done inside a clean room and afterwards it is electrically characterized.
In the beginning, a glass substrate is cut into 25mm∗25mm pieces. Afterwards a thorough cleaning process is performed in which firstly Acetone is used and the glass substrates are immersed in a beaker full of acetone and put inside a ultrasonic bath for 15 minutes and afterwards the same process is repeated using Isopropanol and in the end the glass substrates are dried using a nitrogen gun and stored. In the next step, the source and the drain of the device should be evaporated onto the substrate and for this purpose gold is chosen as the conductive material for the source and the drain electrodes. Using a shadow mask and an evaporation chamber, gold is evaporated onto the glass substrate for the formation of the source and the drain. After a quick inspection, if the formation of the source and drain is satisfactory, the fabrication process can be continued with the deposition of the other layers. For the deposition of other layers, spin coating and annealing is used. For the semiconductor solution, P3HT is dropped onto the glass substrate with the source and drain electrodes. The parameters for the spincoater is as follows: ω = 1000 rpm/sec with an acceleration of 500 rpm/sec for 1 minute. With these parameters, the expected semiconducting layer should have a thickness of 70nm. Afterwards, the spincoated substrate is annealed on a hotplate at 100 °C for 5 minutes.
In the next step, Cytop as the dielectric layer should be applied on top of the semiconducting film which was fabricated in the previous step. For this purpose, 400 µL of cytop is applied on top of the substrate. As for the spincoating parameters, a two step process is used. In the first step, the spincoater has the following parameters: ω = 500rpm with an acceleration of 1000 rpm/sec for 10 seconds to spread the solution and in the second step, ω = 3000rpm, with an acceleration of 1000 rpm/sec for 45 seconds to get to the desired thickness of approximately 650nm. Afterwards, the spincoated substrate is annealed on a hotplate at 100 °C for 5 minutes.
In the final stage of the fabrication process, the gate contact is fabricated and for this process the evaporation chamber is used once more. The substrates are placed onto the sample holder and the samples are covered with a shadow mask. For the gate electrode, a silver source is used to get a 60nm thick silver layer.
The finished device is then characterized electrically in a characterization system that uses three needles to contact the small structures [6]. In which the output characteristic, transfer characteristic, threshold voltage, on/off ratio and field effect mobility of the fabricated devices will be measured by once sweeping the gate voltage while the drain voltage is kept constant and vice versa and all the results will be summarized in the results section.

4 Results

4.1 Transistor Dimensions

A sample array of transistor metal contacts were imaged under a microscope in order to measure the dimensions as shown in Figure 4.1.



(a) (b)

Figure 4.1: Sample transistors with lengths (a) L = 51.0 µm and (b) L = 11.9 µm

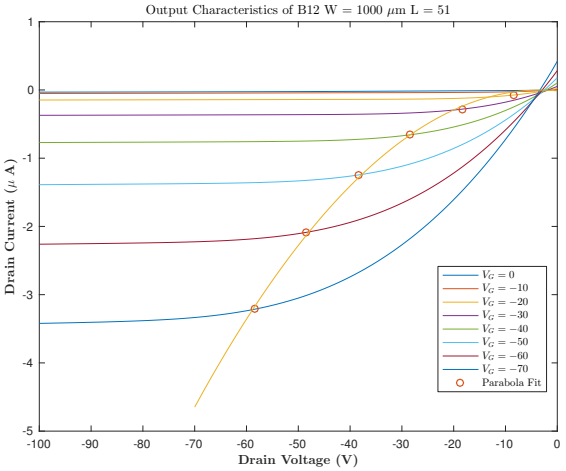
14 different transistor dimensions were measured under the microscope and grouped under 3 different intended lengths. The average values along with standard deviations are shown in table 4.1. The widths of the transistors is consistently at 1025.3 µm while the transistor length changes from 11.9 µm to 22.8 µm to 51.0 µm.
It is observed that the intended length is consistently 1 σ below the measured average which points to a systematic error in either fabrication or measurement.

Intended Lengths	Average Experimental	Standard Deviation
W = 1000 µm	1025.3 µm	29.3 µm
L = 10 µm	11.9 µm	1.9 µm
L = 20 µm	22.8 µm	2.1 µm
L = 50 µm	51.0 µm	1.8 µm

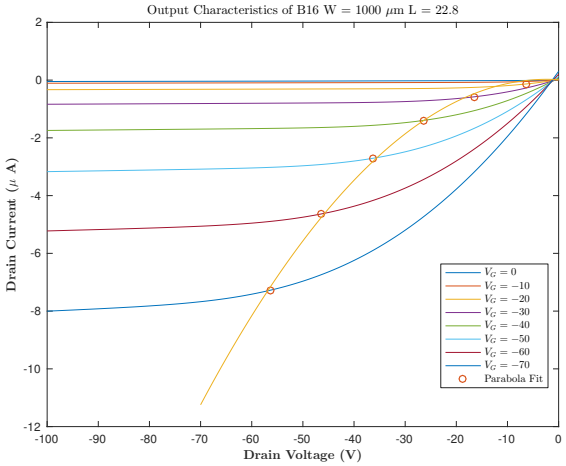
Table 4.1: Measured Average Transistor Dimensions

4.2 Output Characteristics

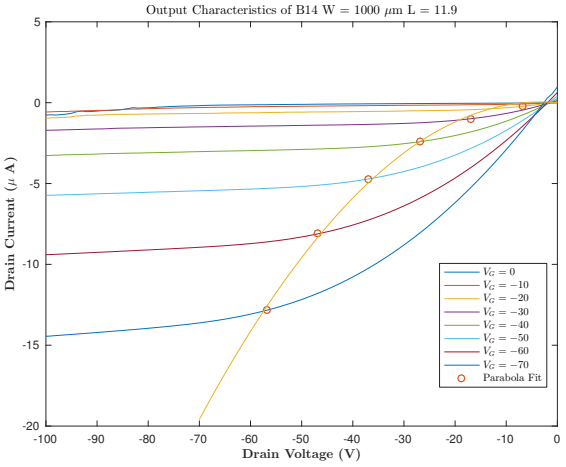
Output characteristics of transistors with different lengths are measured by keeping the gate voltage constant and sweeping the drain voltage as shown in figures 4.2a, 4.2c, 4.2b, and 4.2d. For each curve, the saturation voltage is calculated from $V_{Dsat} = V_G - V_{TH}$ where the threshold voltage is calculated from the corresponding transfer curve. Then through interpolation, the saturation current is calculated from the output curve. The data points for V_{Dsat} vs. I_{Dsat} were fitted to a parabola. As expected, the output currents are smaller for bigger gate lengths. Transistor B14 and C8 have the same geometry in W and L, but differ in the shape of the terminals as one is fatter and shorter while the other thinner but longer yet the channel width comes out to be equal. As they have almost the same output characteristic we can say, that the shape of the terminals is less important for device performance.



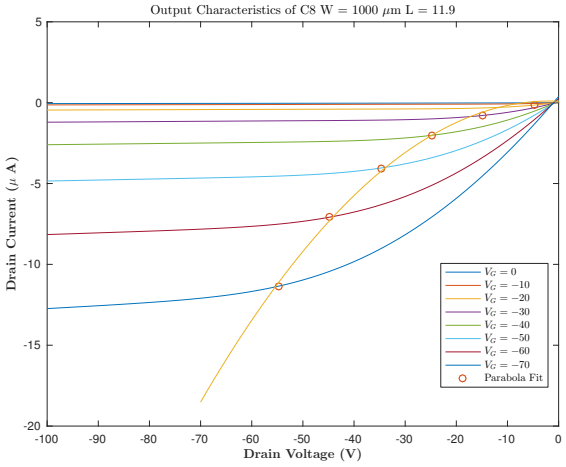
(a) Transistor B12, L = 51.0 µm



(b) Transistor B16, L = 22.8 µm



(c) Transistor B14, L = 11.9 µm

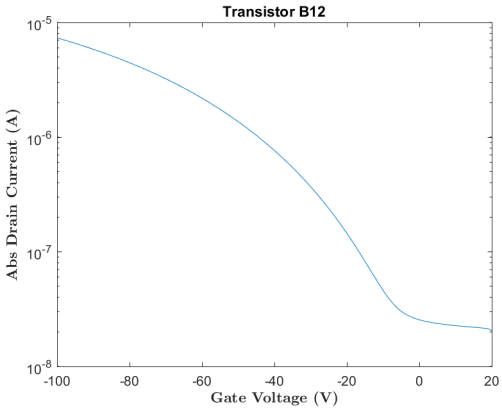


(d) Transistor C8, L = 11.9 µm

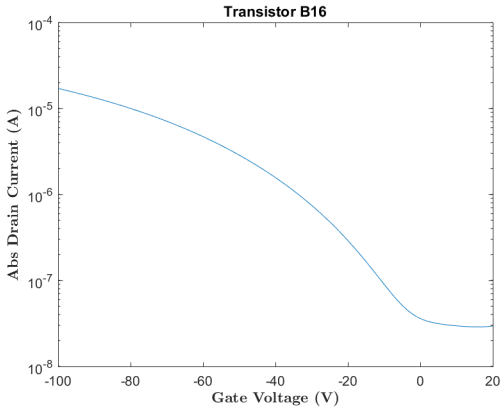
Figure 4.2: Output characteristics of the fabricated transistors. The parabola separates the linear from the saturation regime.

4.3 Transfer Characteristics

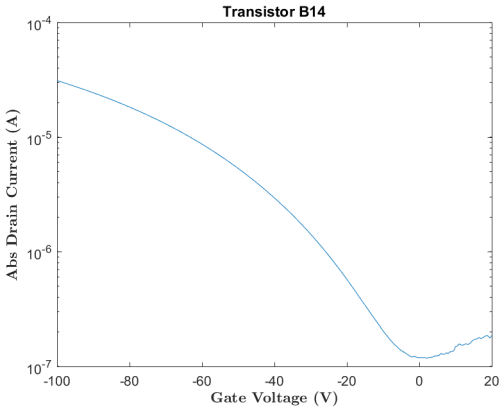
Transfer characteristics were measured by keeping the drain voltage constant (60 V) while varying the gate voltage and measuring the drain current.



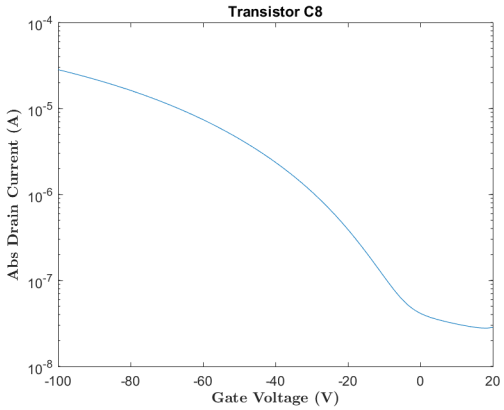
(a) Transistor B12, L = 51.0 µm



(b) Transistor B16, L = 22.8 µm



(c) Transistor B14, L = 11.9 µm



(d) Transistor C8, L = 11.9 µm

Figure 4.3: Transfer Characteristics for the fabricated transistors

Transistors B14 and C8 had the highest drain currents whereas B12 had the smallest current. Transistors with longer gate lengths have larger resistances and therefore smaller currents.

4.3.1 Mobility

Mobility can be calculated from the transistor model. In the linear region [9]:

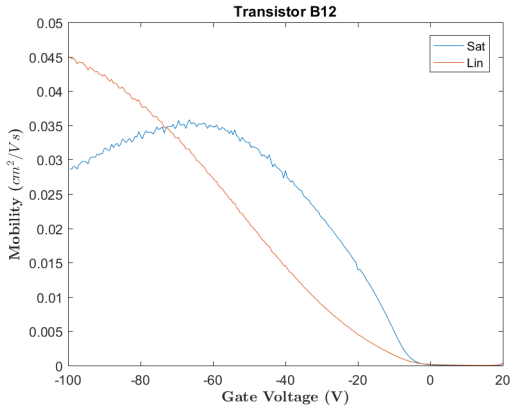
$$\frac{\partial I_{DS}}{\partial V_{GS}} = \mu_{lin} C \frac{W}{L} V_{DS}$$

$$\mu_{lin} = \frac{L}{W} \frac{1}{C V_{DS}} \frac{\partial I_{DS}}{\partial V_{GS}}$$

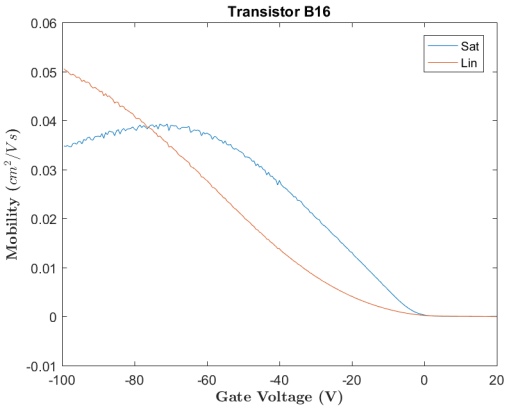
In the saturation region [9]:

$$\mu_{sat} = \frac{2\,L}{W}\frac{1}{C}\left(\frac{\partial\sqrt{I_D}}{\partial V_G}\right)^2$$

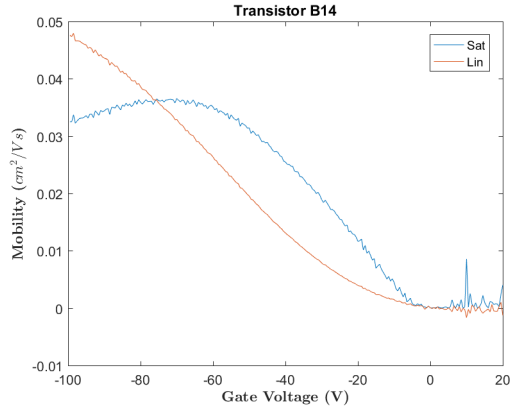
The red curves show the mobility values calculated using the equation for linear regime and the blue one shows that for saturation in Figures 4.5a, 4.5c, 4.5b, and 4.5d. The gate voltage for which the linear regime start can be read from the output curve. For a Drain Voltage of -60V, the transistor is in the saturated regime roughly for gate voltages of -70V and higher.
The oxide capacitance per area is calculated to be 28.6 µFm^{-2} with the following parameters: $\varepsilon_r = 2.1$ for Cytop, $\varepsilon_0 = 8.85410^{-12}$F/m, and oxide thickness $d = 650$nm. V_{DS} is 60 V and the width W is 1025 μm as calculated from the transistor pictures. Forward Euler method was used to calculate the derivatives numerically.



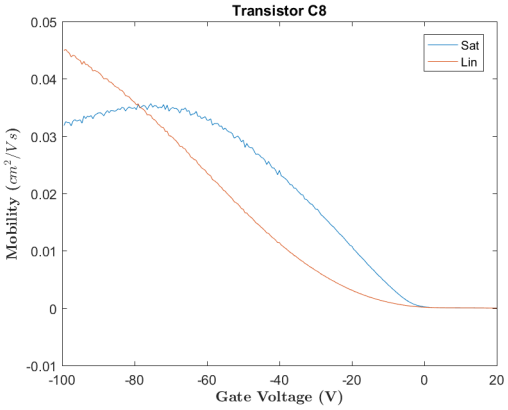
(a) Transistor B12, L = 51.0 µm



(b) Transistor B16, L = 22.8 µm



(c) Transistor B14, L = 11.9 µm



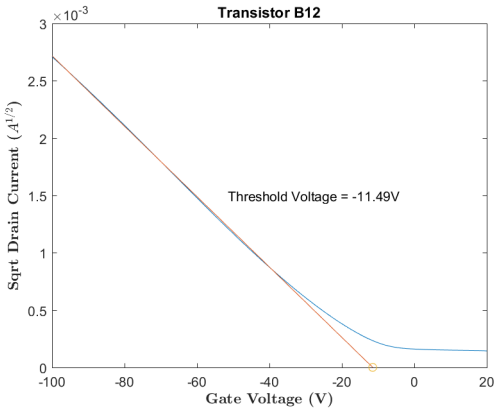
(d) Transistor C8, L = 11.9 µm

Figure 4.4: Mobility for the fabricated transistors

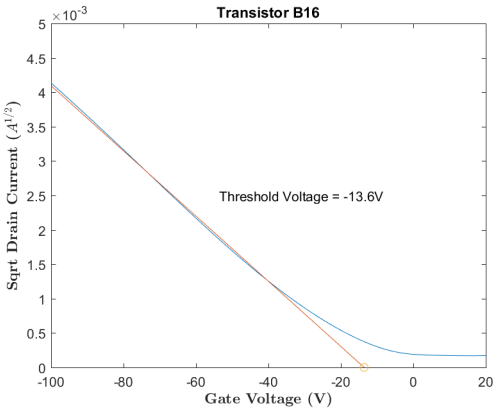
The maximum mobility of the devices does not differ a lot and is around 0.05 cm^2/Vs. This value is in good agreement with those cited in the literature [3].

4.3.2 Threshold Voltage

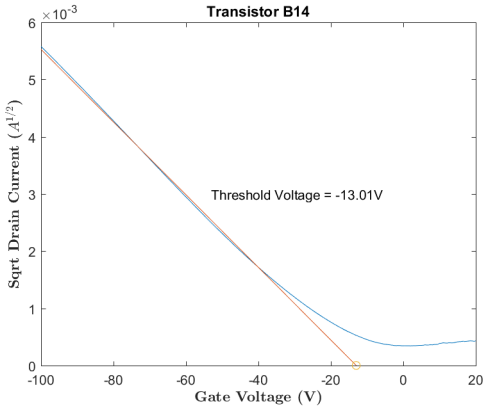
In order to calculate the threshold voltage, square root of the drain current is taken. Then a line is fitted to the region of maximum slope. Threshold voltage is defined as the x-axis (gate voltage) intersection of this line. In Figure 4.5, the maximum slope is roughly between gate voltages of -90V to -30V and a line is fitted to the data points lying in that region.



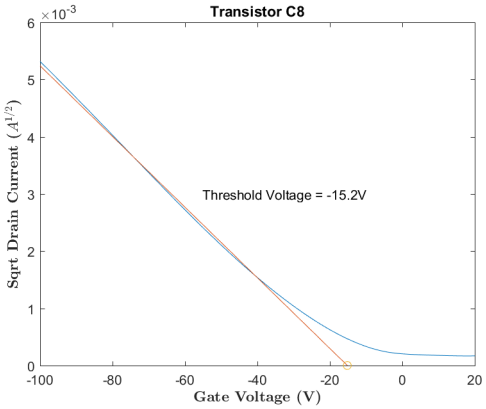
(a) Transistor B12, L = 51.0 µm



(b) Transistor B16, L = 22.8 µm



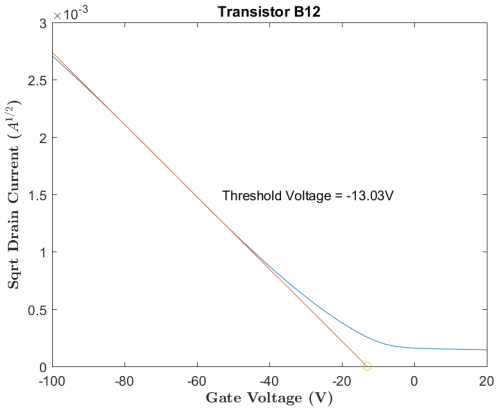
(c) Transistor B14, L = 11.9 µm



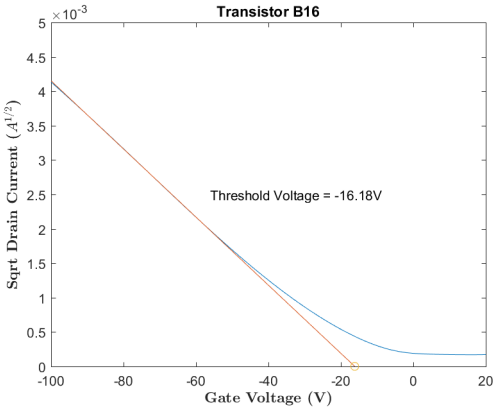
(d) Transistor C8, L = 11.9 µm

Figure 4.5: Transfer characteristic and threshold voltage fitted for data points between -30V and -90V gate voltages

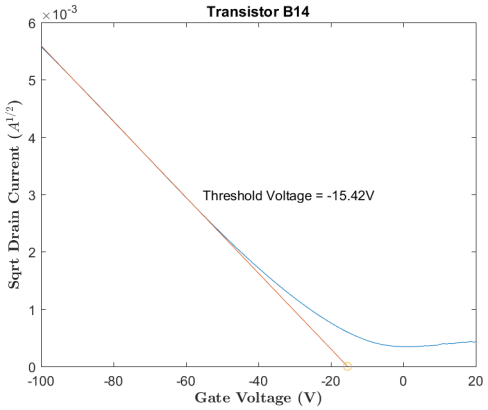
In order to test the validity of the choice of range, for each data set in Figure 4.6 the point of maximum slope is determined by taking a numerical derivative. Then a line is fitted to the data points within $\pm 5\%$ of the value at the point of maximum slope. The range $\pm 5\%$ is randomly chosen and only serves the purpose of comparing different possible methods for calculating the threshold voltage.



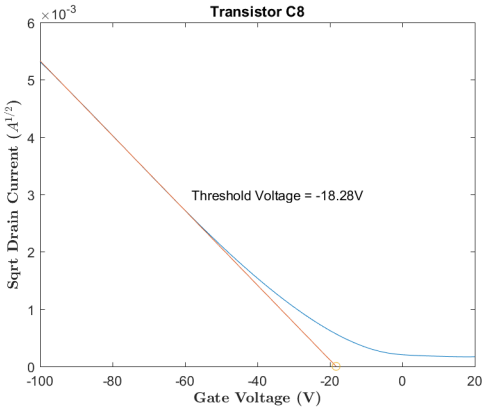
(a) Transistor B12, L = 51.0 µm



(b) Transistor B16, L = 22.8 µm



(c) Transistor B14, L = 11.9 µm



(d) Transistor C8, L = 11.9 µm

Figure 4.6: Transfer characteristic and threshold voltage calculation using data points within $\pm 5\%$ of the maximum slope

Comparing Figures 4.6 and 4.5 shows that the method of choice causes roughly 10% change in the calculated threshold voltage.

4.3.3 On/Off Ratio

The On/Off ratio corresponds to the ratio of the drain current in on state (taken as drain current at -100 V gate voltage) to that in off state (taken as the average current between gate voltages of 0 V and 20 V) at -60V drain voltage. Higher on current corresponds to higher performance and lower off current corresponds to lower leakage. Therefore, a large On/Off ratio is desired. In table 4.2 calculated On/Off ratios are presented.

Transistor	Channel length	On Current (A)	Off Current (A)	On/Off Ratio
B12	51.0 µm	-7.34×10^{-6}	-2.28×10^{-8}	322
B16	22.8 µm	-1.71×10^{-5}	-3.03×10^{-8}	563
B14	11.9 µm	-3.11×10^{-5}	-1.47×10^{-7}	211
C8	11.9 µm	-2.83×10^{-5}	-3.19×10^{-8}	886

Table 4.2: On/Off Current Ratios

Leakage current is expected to be greater for smaller features resulting in smaller on/off ratios. However, the sample set is not large enough to confirm that prediction. It should be noted that B14 has an order of magnitude larger off current resulting in the smallest On/Off ratio. This could be due to higher leakage currents or problems in fabrication (i.e impurities, dislocations, etc). Conversely, transistor C8, which has the same channel length as transistor B14, has the highest On/Off ratio. This might stem from a fatter terminal width, but it is more probable that the differences in On/Off ratio simply come from fabrication inhomogeneities.

5 Conclusion

In the Innovation Lab, several working organic field effect transistors were fabricated in a clean room and electrically characterized. Drain currents in the range of $0.7 - 2.8 \times 10^{-5}$ A were measured from the transfer curves where the current was inversely correlated with gate length at a gate voltage of -100V and drain voltage of -60V. Threshold voltages between 11V and 15V were obtained and on/off ratios between 211 and 886. Maximum mobility is calculated to be around $0.05\,\mathrm{cm}^2/\mathrm{Vs}$. Compared to their inorganic counterparts, fabricated organic transistors have inferior electrical characteristics [9]. Furthermore, electrical characterization and visual inspection of the transistors revealed that those with smaller features are more difficult to manufacture. Therefore, the challenge to fabricate working transistors with small channel lengths still remains.

Bibliography

[1] Zhenan Bao, John A. Rogers, and Howard E. Katz. Printable organic and polymeric semiconducting materials and devices. *Journal Of Materials Chemistry*, (9):1895–1904, 1999.

[2] S. Braun, W.R. Salaneck, and Mats Fahlman. Energy-level alignment at organic/metal and organic/organic interfaces. *Advanced Materials*, 21:1450–1472, 2009.

[3] Jui-Fen Chang, Baoquan Sun, Dag W. Breiby, Martin M. Nielsen, Theis I. Solling, Mark Giles, Iain McCulloch, and Henning Sirringhaus. Enhanced mobility of poly(3-hexylthiophene) transistors by spin-coating from high-boiling-point solvents. *Chem. Mater.*, 16:4772âĂŞ4776, 2004.

[4] I.G. Hill, D. Milliron, J. Schwartz, and A. Kahn. Organic semiconductor interfaces: electronic structure and transport properties. *Applied Surface Science*, (166):354–362, 2000.

[5] Bing Hsieh and Yen Wei. Electroplastic for plastic electronics. *ACS Symposium Series*, 1999.

[6] Light Technology Institute InnovationLab. *Nanotechnology Laboratory, Experiment: Organic Thin-film Transistors*.

[7] Christopher R. Newman, C. Daniel Frisbie, Demetrio A. da Silva Filho, Jean-Luc Bredas, Paul C. Ewbank, and Ket R. Mann. Introduction to organic thin film transistors and design of n-channel organic semiconductors. *Chem. Mater*, (16):4436–4451, 2004.

[8] J. A. Rogers, Z. Bao, H. E. Katz, and Dodabalapur. Thin-film transistors. 377, 2003.

[9] S. M. Sze and Kwok K. Ng. *Physics of Semiconductor Devices*. Wiley-Interscience, 2006.