Electronics for Physicists

Analog Electronics

Chapter 6; Lecture 11

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23.01.2024

KIT, Winter 2023/24

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Chapter 6

2-Transistor Circuits

- Current Mirrors
- Amplifier Circuits

Overview

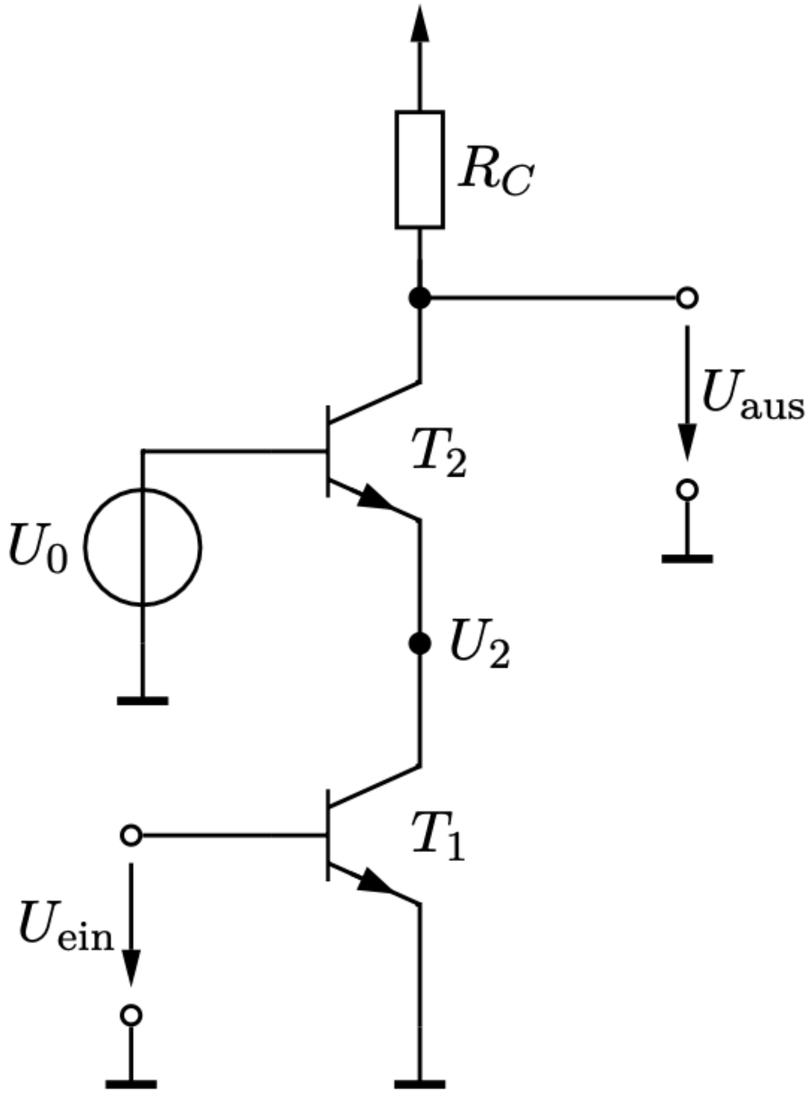
1. Basics
2. Circuits with R, C, L with Alternating Current
3. Diodes
4. Operational Amplifiers
5. Transistors - Basics
6. **2-Transistor Circuits**
7. Field Effect Transistors
8. Additional Topics
   - Filters
   - Voltage Regulators
   - Noise

Amplifiers - Part 2

In: Chapter 6: 2-Transistor Circuits

The Cascode

Kaskoden-Schaltung



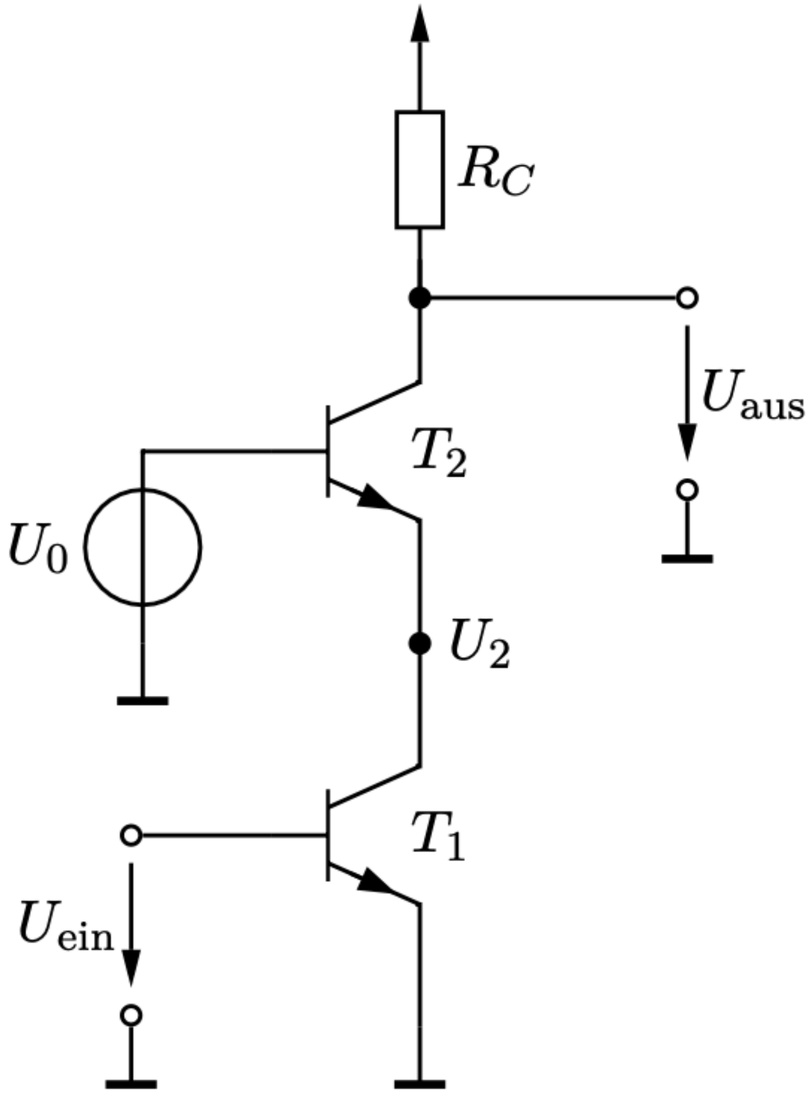
- A very common circuit - cascade of two transistors.
  Features (compared to a single transistor):
  - Better isolation of input and output, with that:
    no Miller effect -> higher bandwidth
  - Higher input impedance
  - Also: higher output impedance

The circuit setup:

- Common emitter with T_1
- Common base with T_2 between T_1 and the collector resistor R_C

The Cascode

Kaskoden-Schaltung



- How the circuit works
  - T_2 as common base amplifier with constant base potential ensures: U_2 relatively constant: U_{E2}, U_{C1}

    ⇨ Almost no voltage amplification in T_1: $dU_2 \sim dU_{ein}$

    Additional consequence: no Miller effect due to C_{BC1}!

How does this provide voltage gain?

Via T_2:

$$V_U = \frac{dU_{aus}}{dU_{ein}} \approx \frac{dU_{aus}}{dU_{U_2}} = SR_C$$

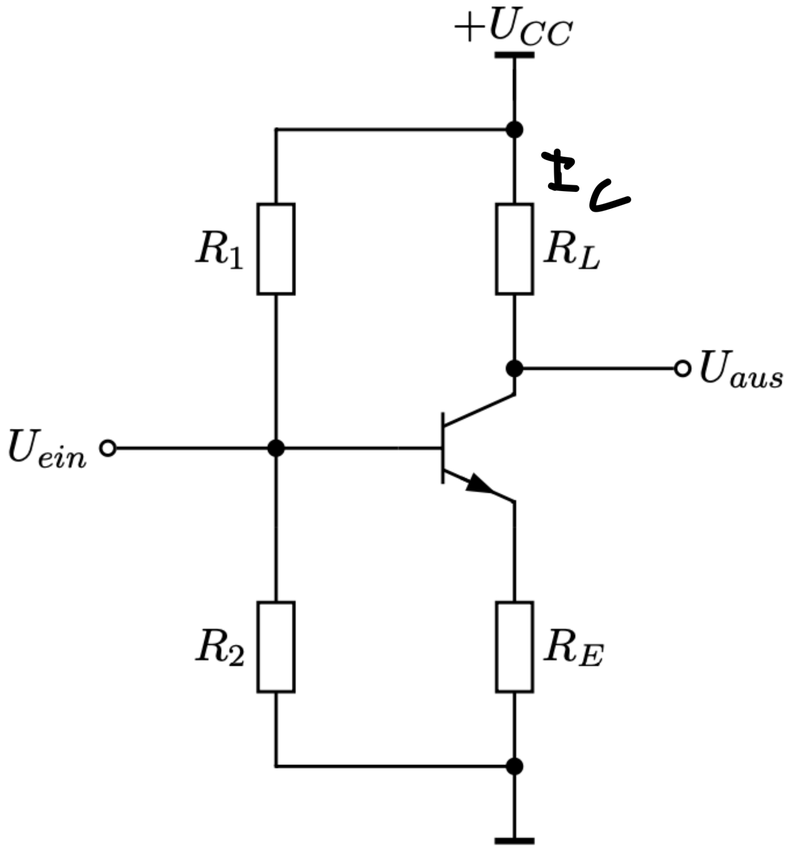
see Ch. 5

Amplifier Classes

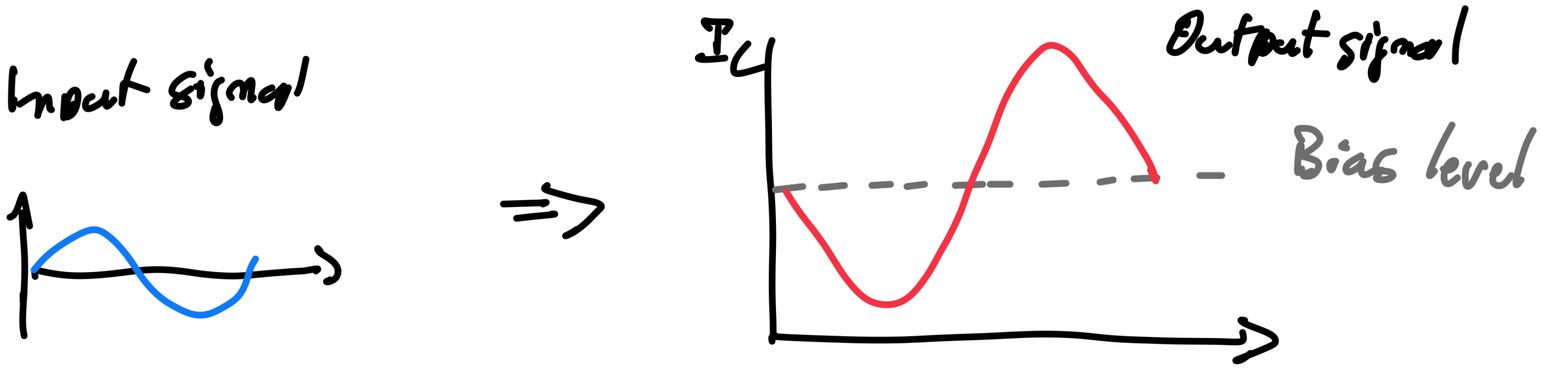
Class A

- Amplifiers are grouped into classes depending on working principle - most common: A, B, AB

Class A



Working point adjusted such that the full signal is amplified: positive and negative half-wave



The Pro: Distortion-free amplification of the full signal.

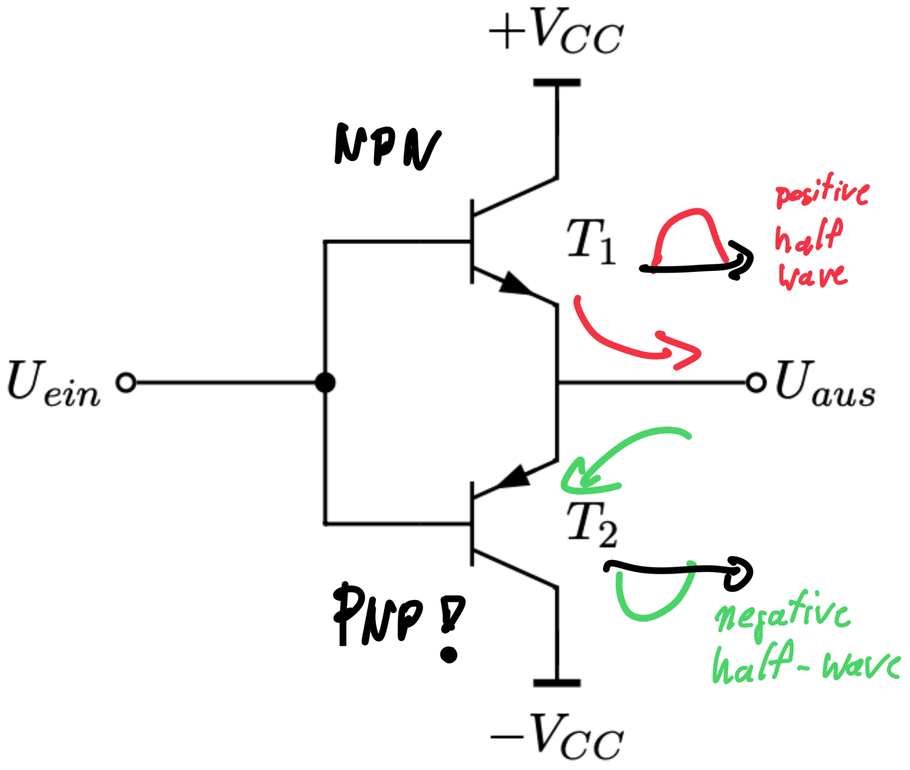
The Con: Low efficiency: Large power also without signal.

Amplifier Classes

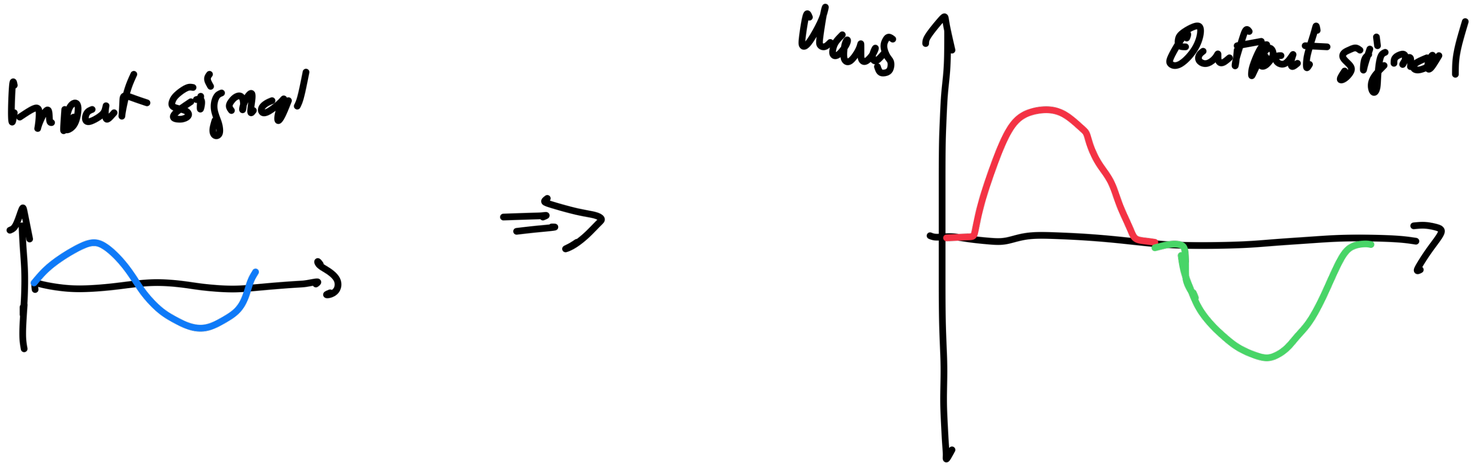
Class B

- Amplifiers are grouped into classes depending on working principle - most common: A, B, AB

Class B



Combination of NPN and PNP transistor - “push-pull amplifier”



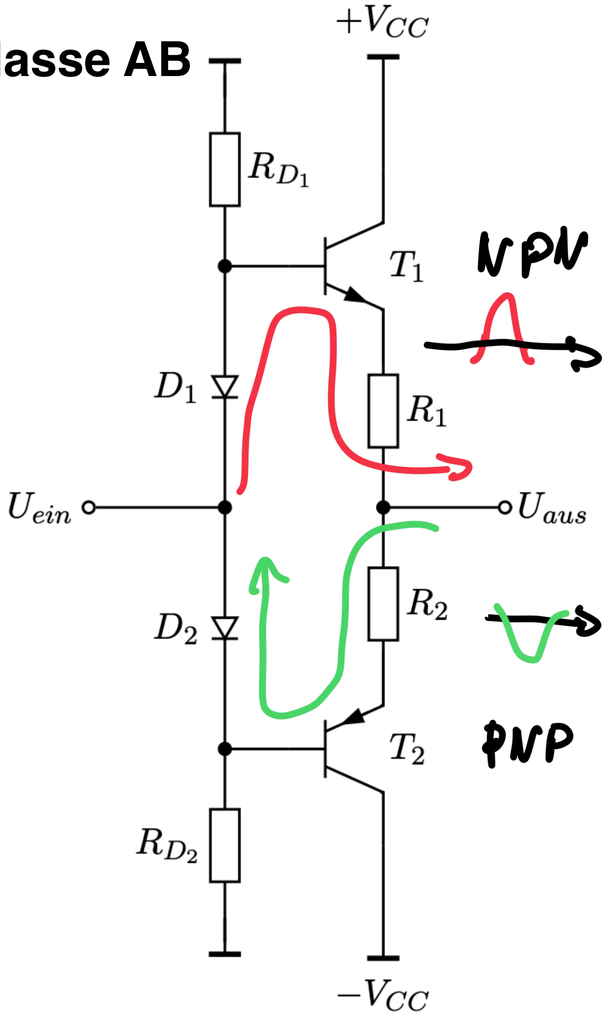
The pros: High energy efficiency - no power w/o signal

The cons: Amplification only for signals $|U_{ein}| > 0.7$ V: Distortion when passing through 0 V, also due to switching between transistors.

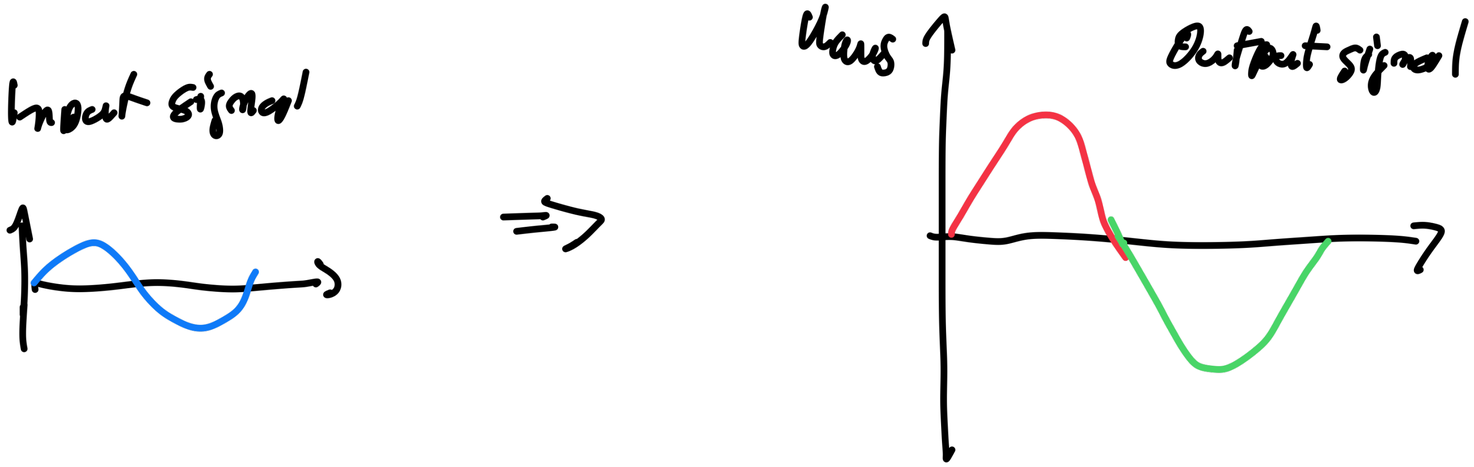
Amplifier Classes

Class AB

- Amplifiers are grouped into classes depending on working principle - most common: A, B, AB



Extension of class B amplifier by adding offset voltages to prevent distortions.



The pros: Good energy efficiency - only small base power, still or only small (or no) distortions.

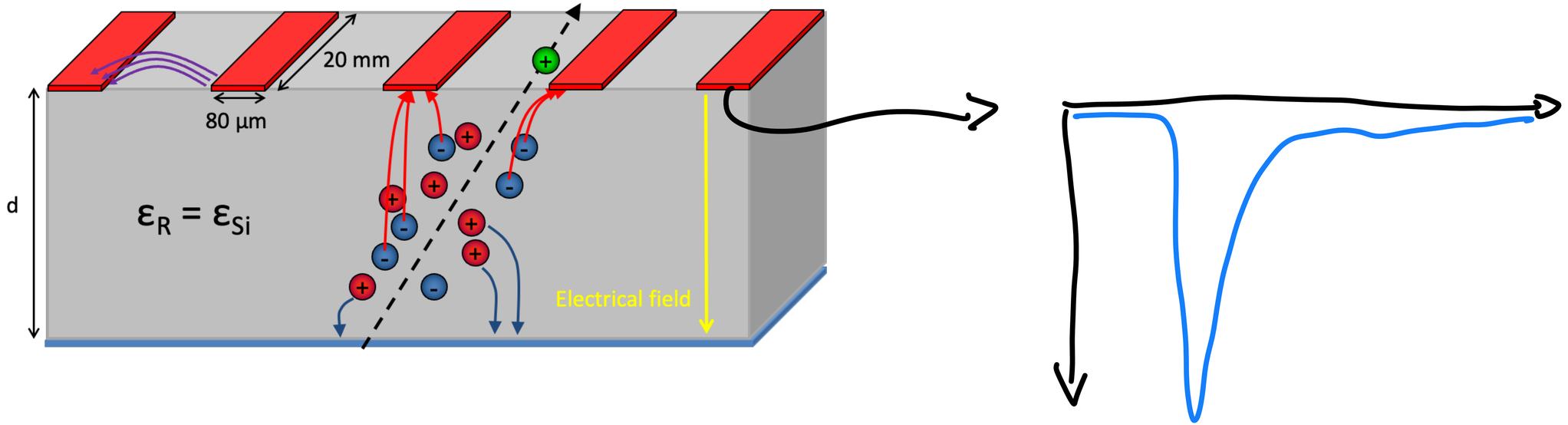
The cons: More complicated than class A (but still small distortions), more power than class B.

Often: The best compromise, for example for audio amplifiers

Amplifier Classes

Perspectives

- Class A well suited for unipolar signals: Working point adjusted such that also small signals are amplified,, but still no (large) current flows w/o signal.



Detector signals normally are unipolar: Class A often suitable.

Different situation: audio signals etc.: Class A for highest quality, but high power.
Class AB or B depending on willingness for compromises.

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Chapter 7

Field Effect Transistors

- MOSFET Basics
- Excursion: CMOS Technology
- CMOS Circuits

Overview

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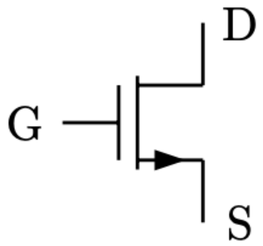
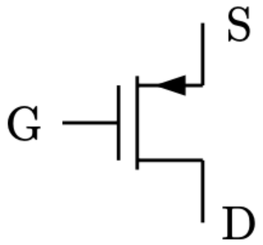
Field Effect Transistors

Introduction

- Two basic types:
  - Metal Oxide Semiconductor Field Effect Transistor (MOSFET)
  - Junction Field Effect Transistor (JFET)

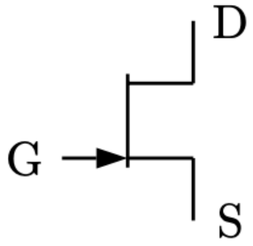


NMOS

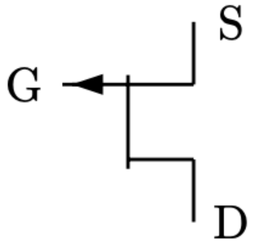


PMOS

MOSFET



n-Kanal



p-Kanal

JFET

Gate
Source
Drain

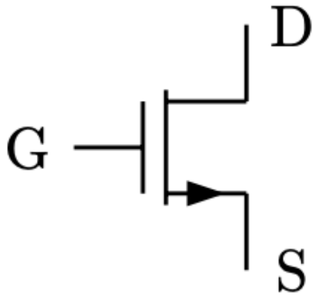
MOSFETs are the most common transistors -> Our focus here!

MOSFET Basics

In: Chapter 7: Field Effect Transistors

FETs in MOS Technology

NMOS FET

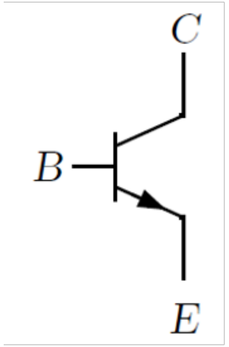


The voltage at the gate U_{GS} defines the current flow between drain und source

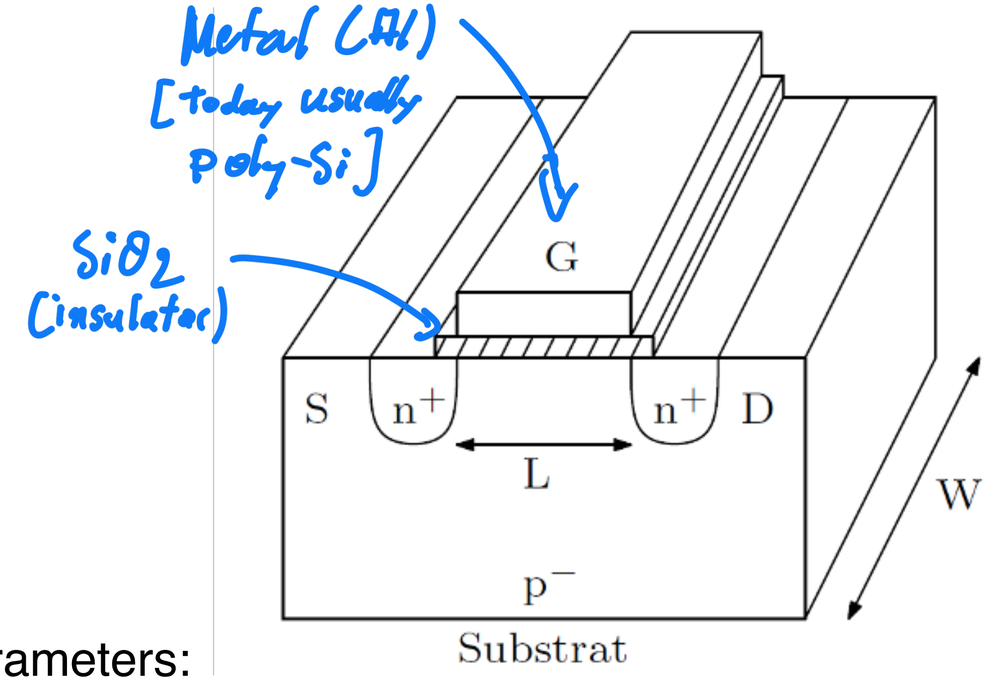
⇨ Voltage-driven current source

No current flow from G to S (with AC input there is a gate current due to charging / discharging of the gate capacity)

Significantly different from BJT:



Current-driven current source, current from base to emitter

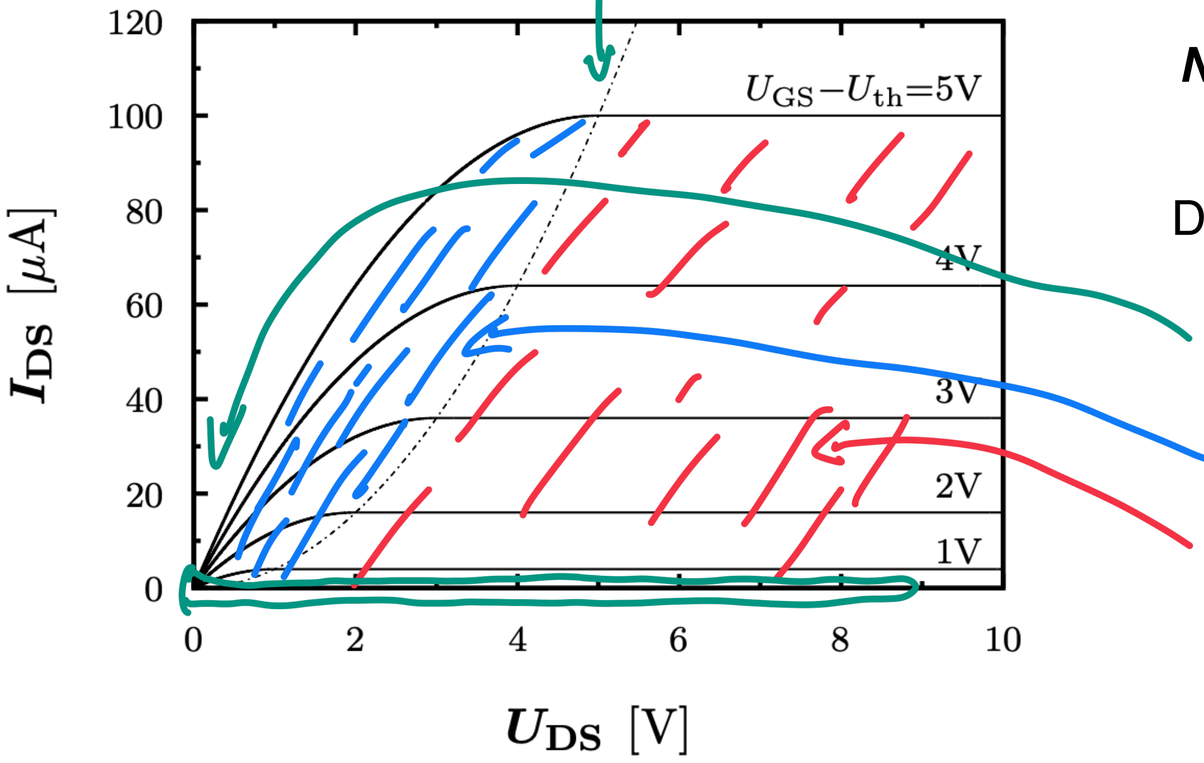


- Parameters:
  - Substrate thickness: typ. ~ 700 μm
  - Gate length L: Defined by technology - for example 22 nm, or 250 nm
  - Gate thickness: Defined by technology gegeben - zB 1 nm or 5 nm
  - Width W: Choice of the designer, but W ≥ L

FET IV Curves

Kennlinien

Transition from linear - saturation
($U_{DS} = U_{GS} - U_{th}$)



U_{th}: Transistor=dependent threshold voltage (a few 100 mV)

- Drain-source current I_{DS} as function of U_{DS} for different gate voltags U_{GS}
  - Requires $U_{DS} > 0$ and $U_{GS} > U_{th}$ for current clow.

NMOS - Transistor

Distinguishing three different regions

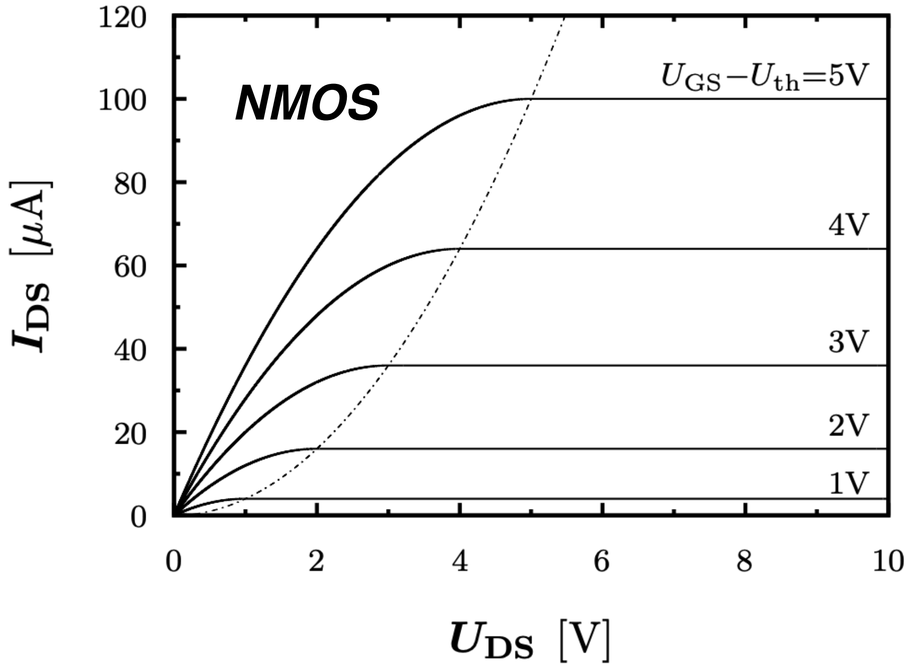
- „Cut-off“ or „weak inversion“ ($U_{GS} < U_{Th}$)
- Linear or ohmic region
- „Strong inversion“ or saturation region

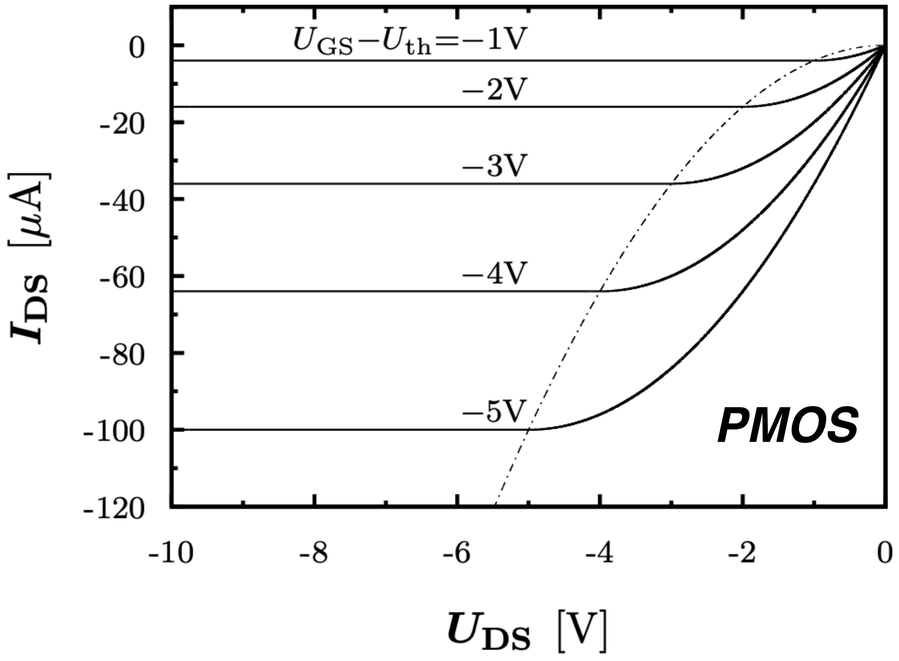
NB: The nomenclature is a bit confusing: For MOSFETs the saturation region corresponds to large U_{DS}, for BJTs it is small U_{CE}

FET IV Curves

NMOS and PMOS

- Drain-Source current I_{DS} as a function of U_{DS} for different gate voltages U_{GS}

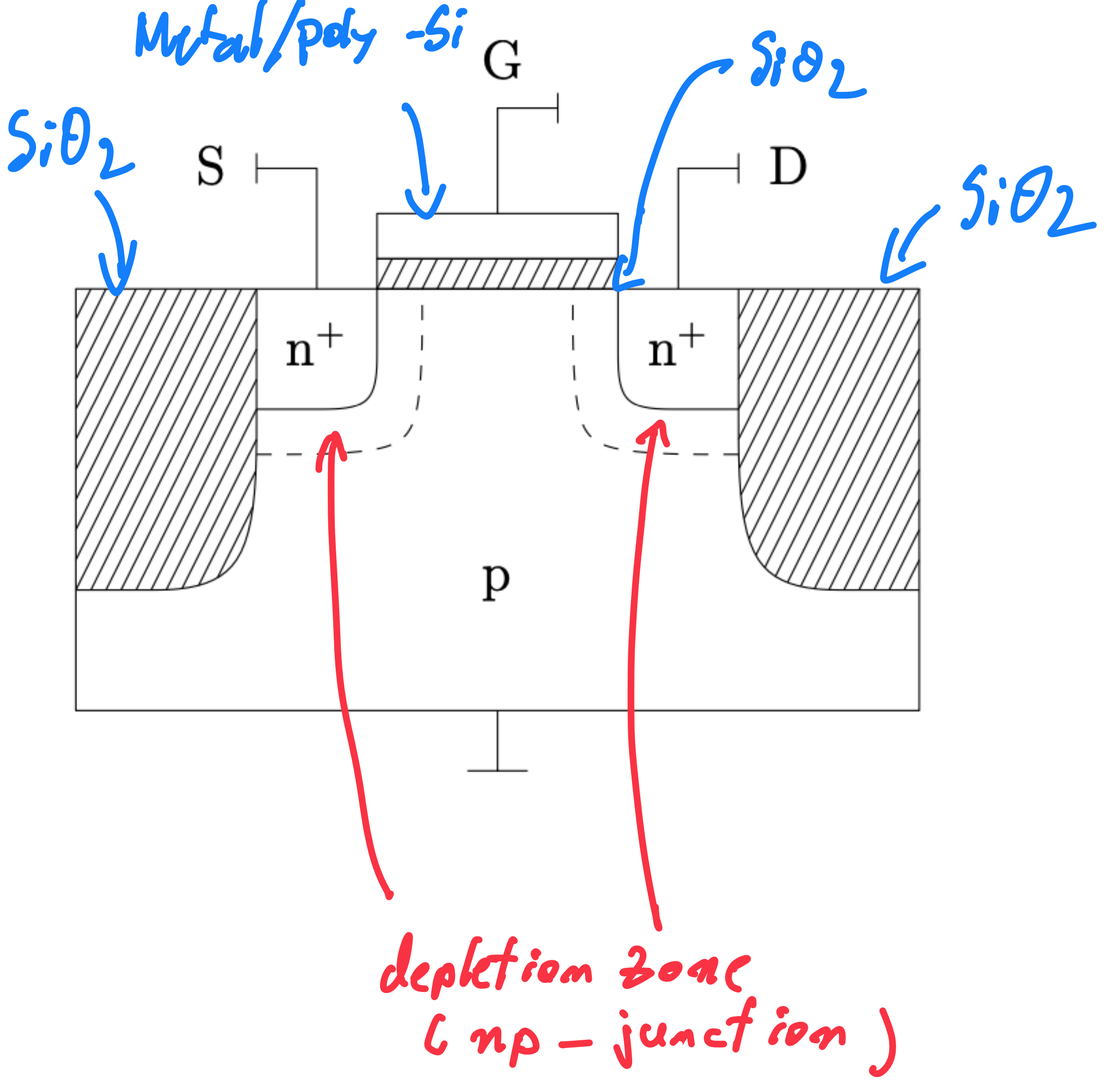




Just as for the BJT transconductance is defined as: $g_m = \frac{dI_{DS}}{dU_{GS}}$ *Steilheit*

FET Operating Principle - NMOS

Cut-off / Weak Inversion



- Cut-off (*Sperr-Bereich, Unterschwellenbereich*):
  $U_{GS} < U_{th}$

  leakage current (sub-threshold current)

  due to thermal excitation:

$$I_{DS} = I_{DS_0}\, e^{\frac{U_{GS} - U_{Th}}{n\, U_T}}$$ as for diodes: n > 1

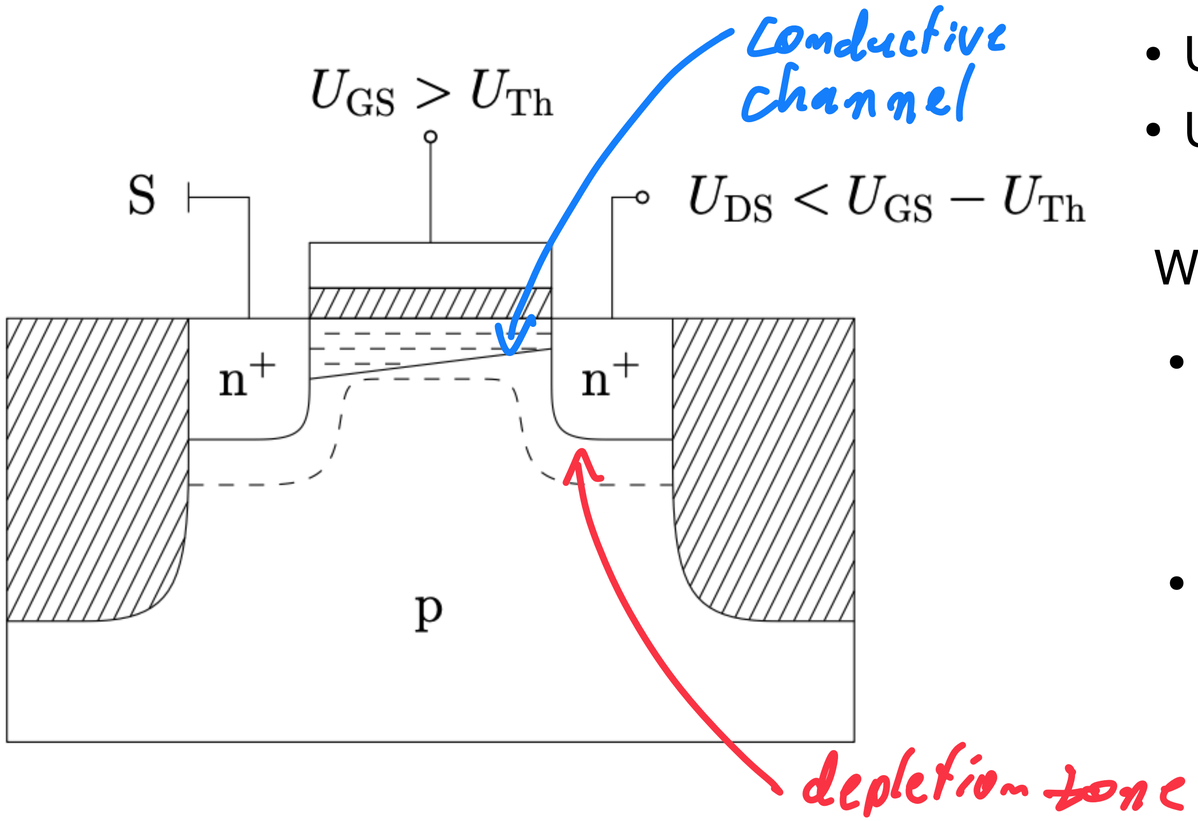
$$I_{DS_0} = I_{DS}(U_{GS} = U_{Th})$$

Transconductance: $g_m = I_{DS}\frac{q_e}{nk_BT}$

In general: a rare operating mode - for example for applications with extremely low power.

FET Operating Principle - NMOS

Linear / Ohmic Region



- $U_{GS} > U_{Th}$: transistor switched “conductive”
- $U_{DS} < U_{GS} - U_{Th}$

What is happening:

- Conductive channel under gate with free neg. charge carriers: Inversion charge (holes are pushed out)
  - U_{GS} determines the available charge
- Voltage between source and drain U_{DS} results in current flow via free charge carriers in channel

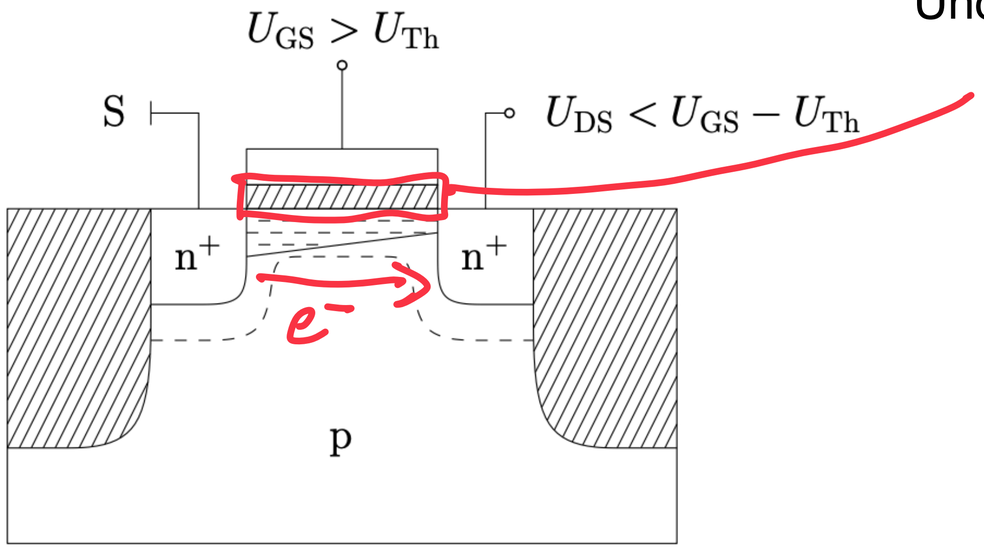
Current between drain and source:

$$I_{DS} = \beta \left[U_{GS} - U_{Th} - \frac{U_{DS}}{2} \right] U_{DS}$$

⇨ Behaves as a ohmic resistor controlled via U_{GS}.
(NB: β not the same as for BJT)

FET Operating Principle - NMOS

Linear Region - Derivation



Understanding the working principle:

Considering the gate as a capacitor:

Surface charge: $Q_F = C_{Ox} \cdot (U_{GS} - U_{Th})$ (for $U_{DS} = 0$)

with $C_{Ox} = \epsilon_0 \epsilon_{SiO_2} \frac{1}{d_{Ox}}$ ($\varepsilon_{SiO2} \sim 11.9$)

For $U_{DS} > 0$: $Q_F = C_{Ox} \cdot (U_{GS} - U_{Th} - U(x))$

(U(x) Voltage between source and position x in channel)

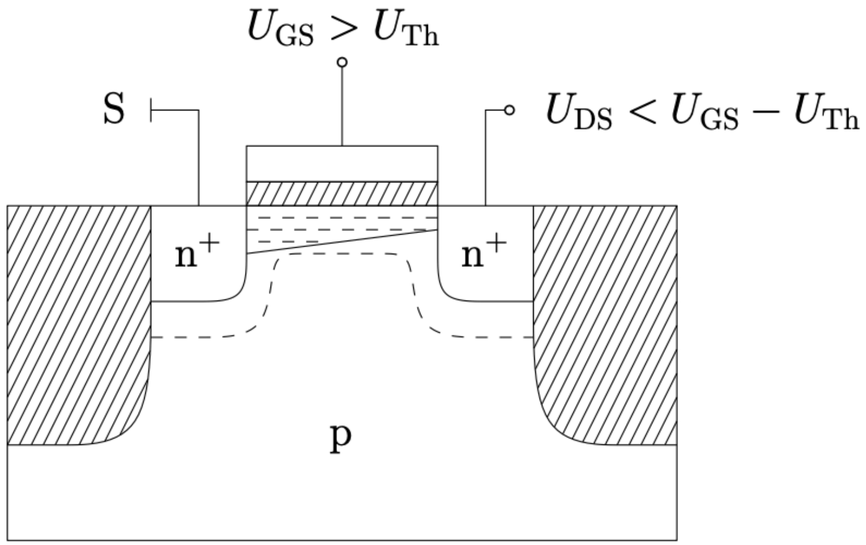
Current between source and drain due to free charges, which are drifting in the field created by the voltage:

given by mobility of the charge carriers μ: $v_D = \frac{dx}{dt} = \mu E_{Drift} = \mu \frac{U_{DS}}{L}$, also: $v_D = \mu \frac{dU(x)}{dx}$

In Si: holes ~ 450 cm²/Vs, electrons ~ 1400 cm²/Vs

FET Operating Principle - NMOS

Linear Region - Derivation



Understanding the working principle - Part II:

Current via moving charge:

$$I_{DS} = \frac{dQ}{dt} = Q_F W \frac{dx}{dt}$$ (W: with of the channel / gate)

$$\Rightarrow \quad I_{DS} = C_{Ox} W (U_{GS} - U_{Th} - U(x)) \mu \frac{dU(x)}{dx}$$

Integration over the full length of channel / gates (= from 0 to U_{DS}) :

$$I_{DS} \int_0^L dx = I_{DS} L = \mu C_{Ox} W \int_0^{U_{DS}} (U_{GS} - U_{Th} - U(x)) dU =$$

$$= \mu C_{Ox} W (U_{GS} - U_{Th}) U_{DS} - \frac{U_{DS}^2}{2}$$

Results in:

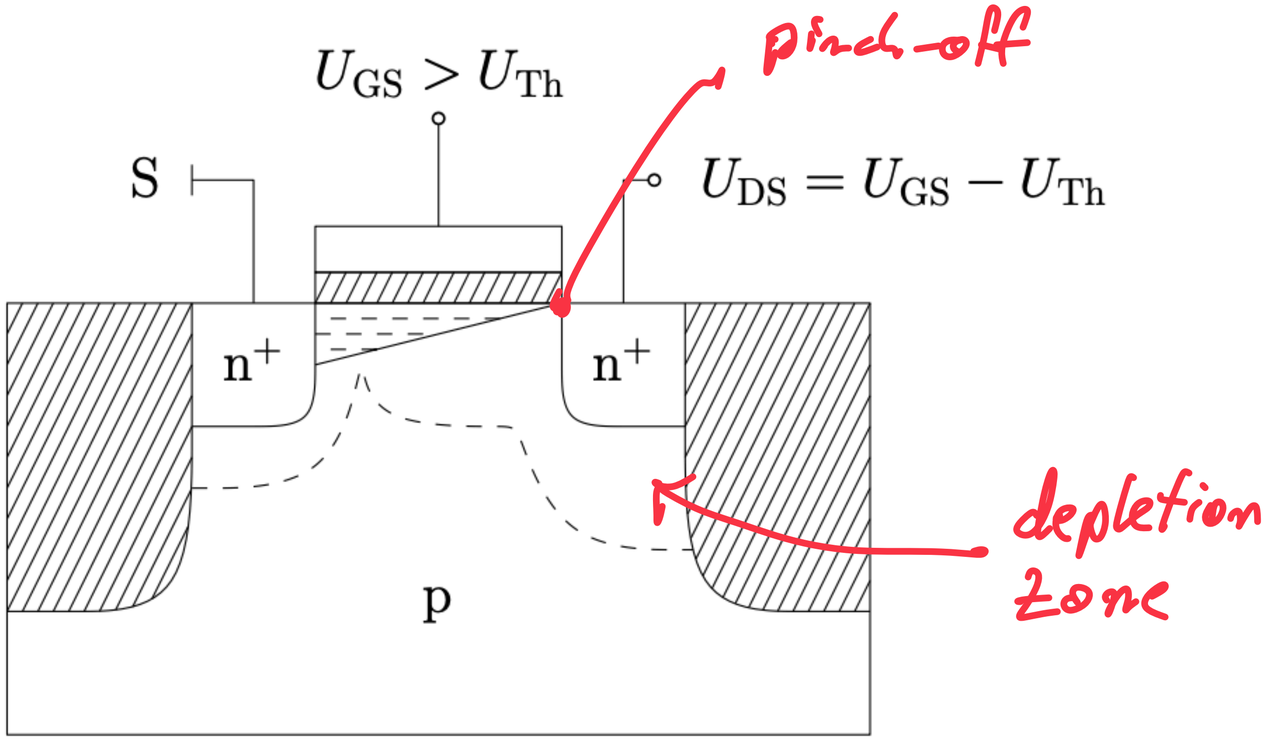
$$I_{DS} = \mu C_{Ox} \frac{W}{L} (U_{GS} - U_{Th}) U_{DS} - \frac{U_{DS}^2}{2}$$

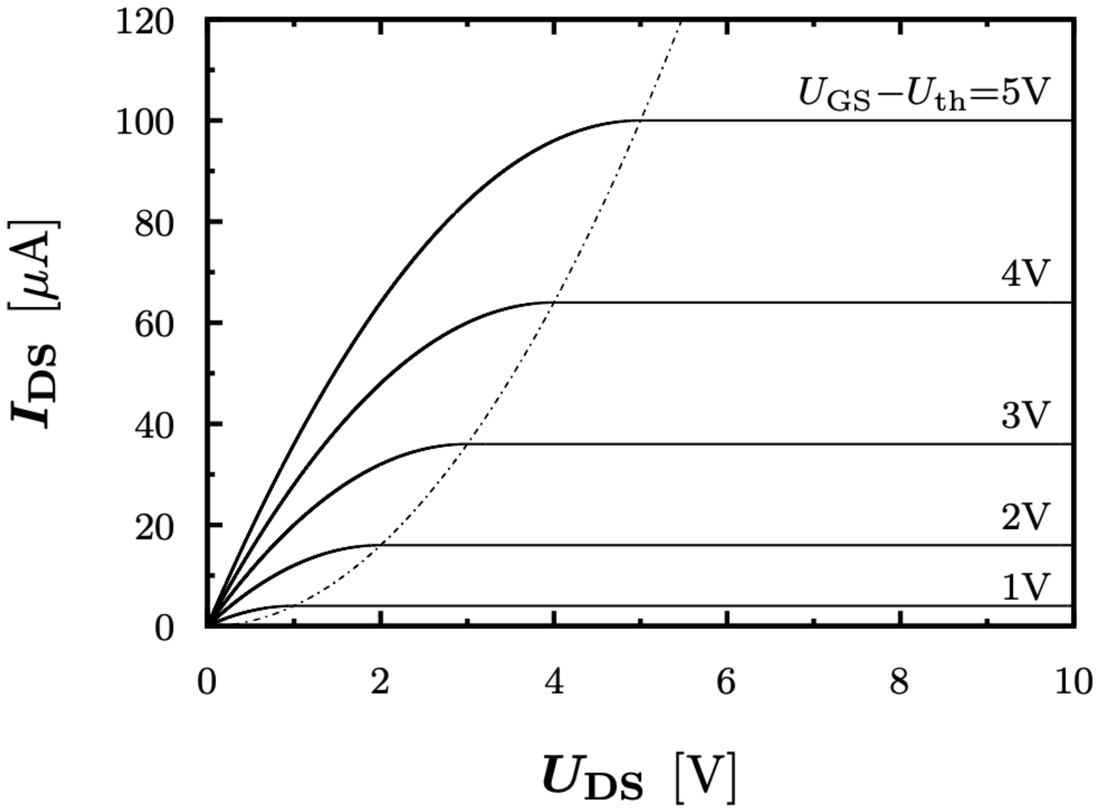
$$I_{DS} = \beta \left(U_{GS} - U_{Th} - \frac{U_{DS}}{2}\right) U_{DS}$$

Defines transconductance coefficient $\beta = \mu C_{Ox} \frac{W}{L}$

FET Operating Principle - NMOS

Strong Inversion

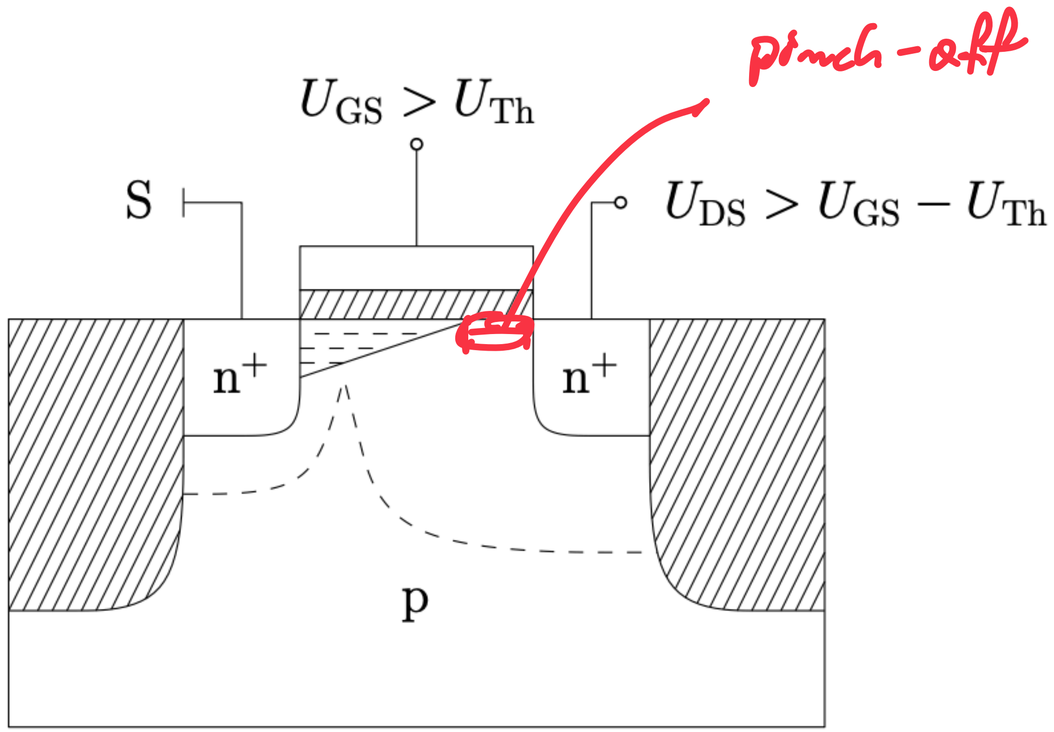




- Pinch-off of the channel on the drain side (“*abschnüren*”)

FET Operating Principle - NMOS

Strong Inversion



- With increasing voltage U_{DS}:
  Stronger pinch-off, resulting in reduced surface area in channel and reduced number of charge carriers, simultaneous increase of voltage: no further increase in current => **saturation**

- Conduction through depletion zone: Electrons from the channel are “drained” into the drain

Behavior now defined by the saturation voltage (determines channel length): $U_{DS_{sat}} = U_{GS} - U_{Th}$

Transconductance: $g_m = \beta\,(U_{GS} - U_{Th}) = \sqrt{2\beta\, I_{DS}}$

and: $\frac{g_m}{I_{DS}} = \frac{2}{U_{GS} - U_{Th}}$

$$I_{DS} = \beta\,(U_{GS} - U_{Th} - \frac{U_{DS_{sat}}}{2})\,U_{DS_{sat}} = \frac{\beta}{2}(U_{GS} - U_{Th})^2$$

=> I_{DS} independent from U_{DS}

the most common operational mode of MOSFETS

FET Operating Principle - NMOS

Summary

Region	**weak inversion** $U_{GS} < U_{Th}$	**linear region** $U_{GS} > U_{Th},\ U_{DS} < U_{GS} - U_{Th}$	**strong inversion** $U_{GS} > U_{Th},\ U_{DS} \geq U_{GS} - U_{Th}$
I_{DS}	$I_{D_0}\, e^{\frac{U_{GS}-U_{Th}}{n\,U_T}}$	$\beta \left[U_{GS} - U_{Th} - \frac{U_{DS}}{2}\right] U_{DS}$	$\frac{\beta}{2}\,(U_{GS} - U_{Th})^2\,(1 + \lambda\, U_{DS})$
g_m	$I_{DS}\,\frac{q_e}{n\,k\,T}$	$\beta\, U_{DS}$	$\sqrt{2\,\beta\, I_{DS}}$

g_m - transconductance

$g_{DS} = 1/R_{DS}$

$$g_m = \frac{dI_{DS}}{dU_{GS}}$$

- In reality: Slight deviation from idealized behavior discussed on the previous slides:

  Early Effect also for FETs: Mild dependence of current on U_{DS} in saturation region due to pinch-off, resulting in $g_{DS} \neq 0$. With that:

$$I_{DS} = \frac{\beta}{2}\,(U_{GS} - U_{Th})^2\,(1 + \lambda U_{DS})$$

$\lambda \sim 0.01$ - $0.1\ V^{-1}$

and:

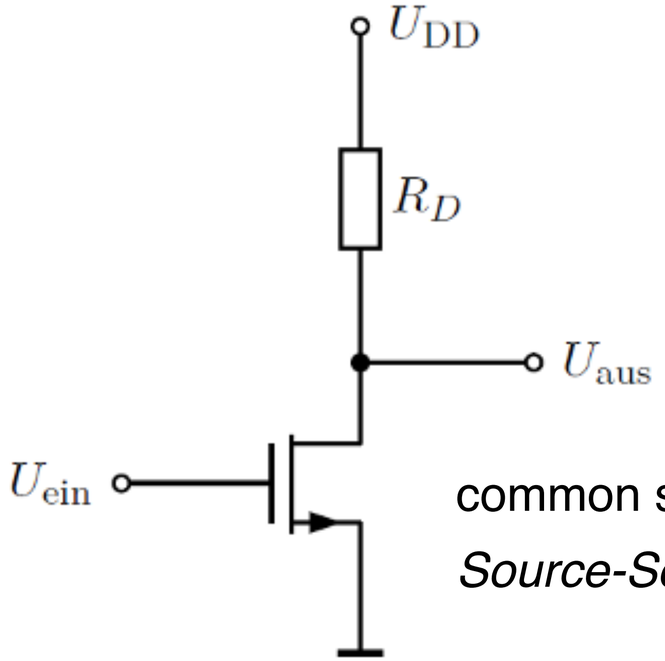
$$g_{DS} = \frac{dI_{DS}}{dU_{DS}} = \frac{\lambda I_{DS}}{1 + \lambda U_{DS}} \sim \lambda\, I_{DS}$$

CMOS Circuits

In: Chapter 7: Field Effect Transistors

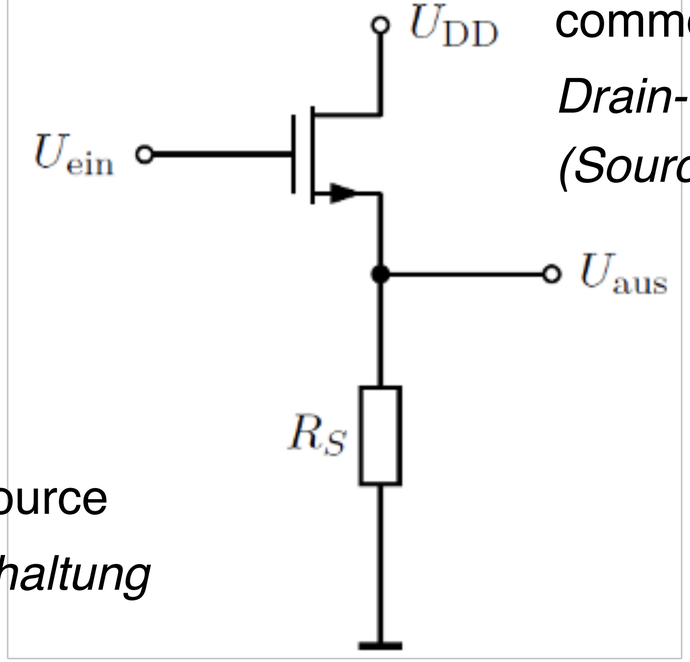
CMOS Basic Circuits

Analoguous to BJT



common source

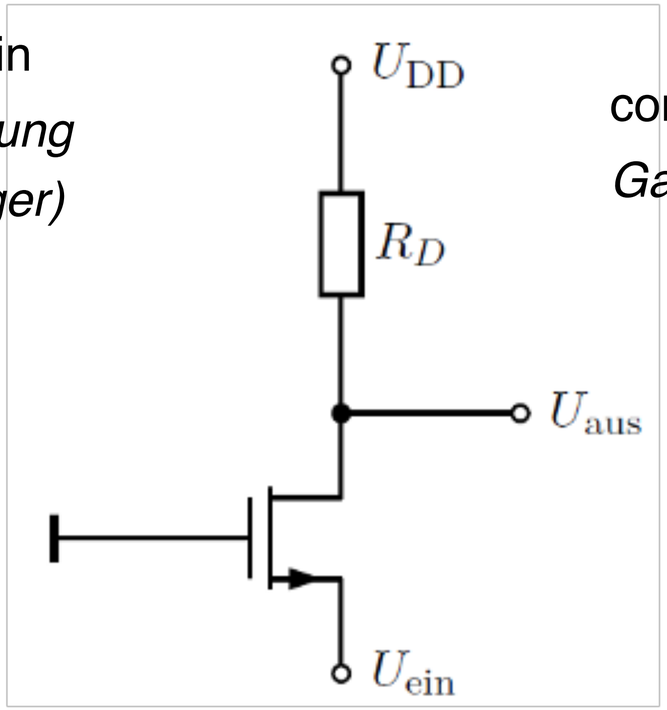
Source-Schaltung



common drain

Drain-Schaltung

(Source-Folger)



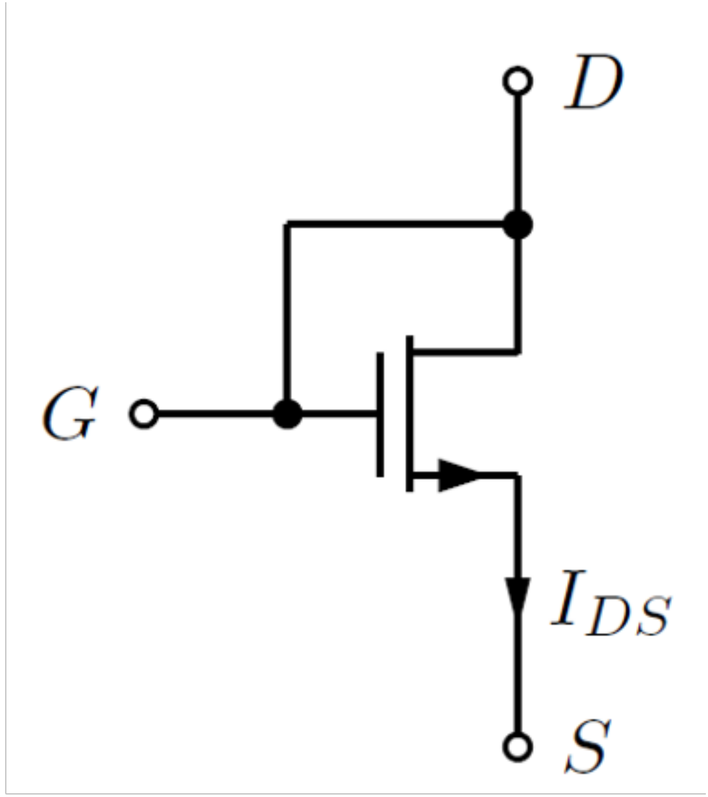
common gate

Gate-Schaltung

Eigenschaften	Sourceschaltung	Drainschaltung	Gateschaltung
Eingangsimpedanz	sehr hoch	sehr hoch	klein, $Z_{ein} \approx \frac{1}{g_m}$
Ausgangsimpedanz	$Z_{aus} \approx R_D$	„klein“, $Z_{aus} \approx \frac{1}{g_m} \parallel R_S$	$Z_{aus} \approx R_D$
Spannungsverstärkung	$V_U = -R_D\, g_m$	$V_U \approx 1$	$V_U \approx R_D\, g_m$

FET as a Diode

NMOS configured as a diode



- For positive U_{DS}:

$$U_{DS} = U_{GS} \geq U_{GS} - U_{Th}$$ (as long as $U_{GS} > U_{Th}$)

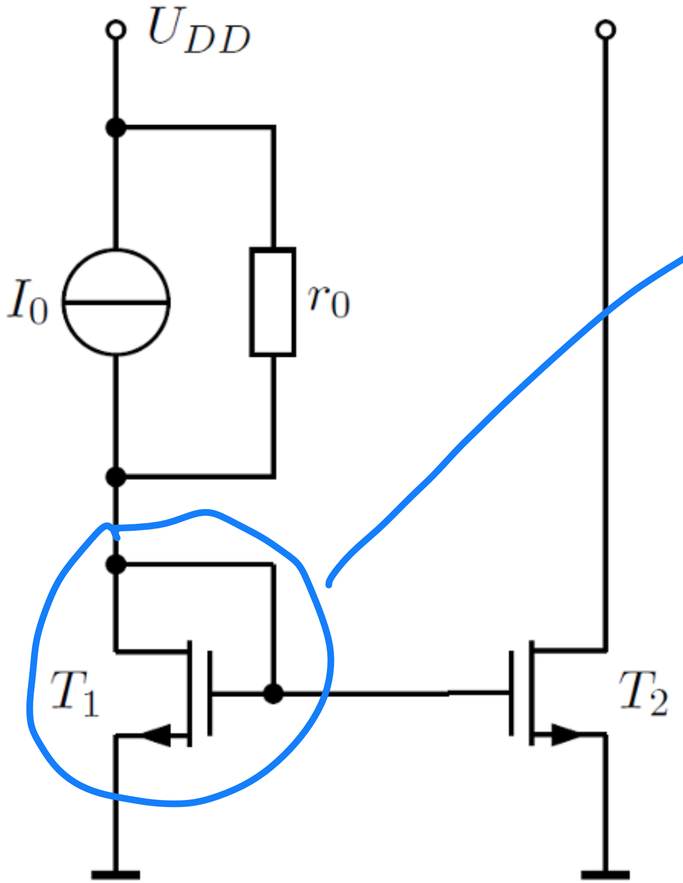
Operation in saturation region, transistor conductive.

- For negative U_{DS}: transistor in reverse bias

Differential source-drain resistance:

$$r_{DS} = \frac{\partial U_{DS}}{\partial I_{DS}} = \frac{\partial U_{GS}}{\partial I_{DS}} = \frac{1}{g_m}$$

Current Mirror with FETs



Principle:

reference current through T_1

FET diode: $\Delta U = U_{GS1} = I_1 \cdot r_{DS} = \frac{I_1}{g_{m1}}$

In the saturation region: $g_m = \sqrt{2\beta I_{DS}}$

$\Rightarrow U_{GS1} = \frac{I_1}{\sqrt{2\beta_1 I_1}} = \sqrt{\frac{I_1}{2\beta_1}}$ $\qquad \beta = \mu C_{ox} \frac{W}{L}$

$U_{GS1} = U_{GS2}$

$\Rightarrow \frac{I_1}{2\beta_1} = \frac{I_2}{2\beta_2} \Rightarrow \frac{I_1}{I_2} = \frac{\beta_1}{\beta_2} = \frac{W_1 L_2}{W_2 L_1}$

Next Lectures:

- Digital - Thursday, January 25
- Analog 12 - Chapter 07 - Tuesday, January 30, 2024

Time Plan for Next Lectures

A few Changes coming up!

Calender Week	Tuesday	Thursday
45	07.11. **Analog**	09.11. **Digital**
46	14.11. **Analog**	16.11. **Digital**
47	21.11. **Digital**	23.11. **Analog**
48	28.11. **Digital**	30.11. **Digital**
49	05.12. **Digital**	07.12. **Analog**
50	12.12. **Digital**	14.12. **Analog**
51	19.12. **Analog**	21.12. **Digital**
2	09.01. **Analog**	11.01. **Digital**
3	16.01. **Digital**	18.01. **Digital**
4	23.01. **Analog**	25.01. **Digital**
5	30.01. **Analog**	01.02. **Digital**
6	06.02. **Analog**	08.02. **Analog**
7	13.02. **Analog**	15.02. **Digital**

Electronics for Physicists

Analog Electronics

Frank Simon
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Karlsruhe Institute of Technology

KIT, Winter 2023/24

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