Electronics for Physicists

Analog Electronics

Chapter 7; Lecture 12

Frank Simon
Institute for Data Processing and Electronics

30.01.2024

KIT, Winter 2023/24

Karlsruhe Institute of Technology

Institute for Data Processing and Electronics

Chapter 7

Field Effect Transistors

- MOSFET Basics
- Excursion: CMOS Technology
- CMOS Circuits

Overview

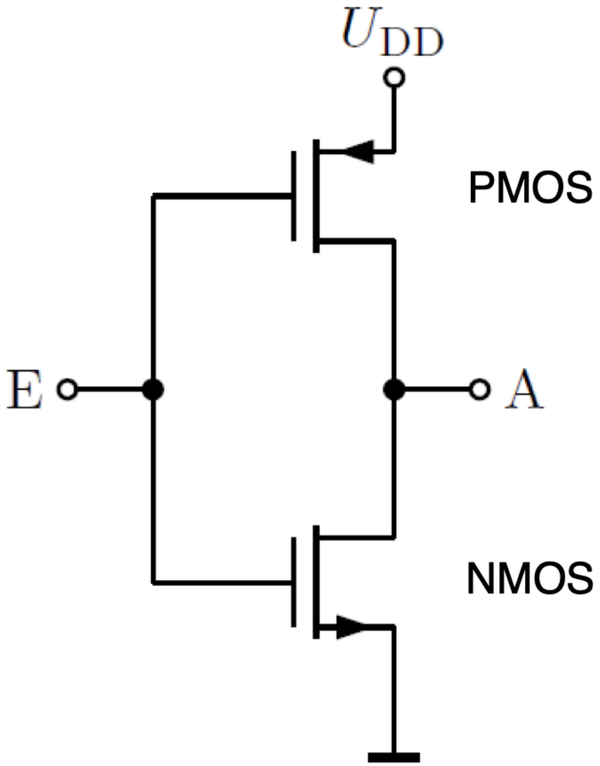
1. Basics
2. Circuits with R, C, L with Alternating Current
3. Diodes
4. Operational Amplifiers
5. Transistors - Basics
6. 2-Transistor Circuits
7. **Field Effect Transistors**
8. Additional Topics
   - Filters
   - Voltage Regulators
   - Noise

Excursion: CMOS Technology

In: Chapter 7: Field Effect Transistors

- **CMOS**: *Complementary Metal-Oxide Semiconductor*
  Uses pairs of NMOS and CMOS - elements to build logic functions

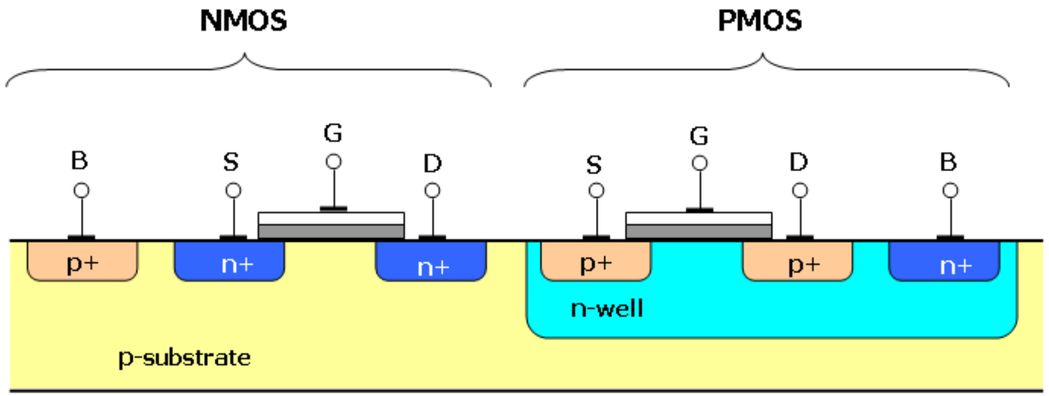
An Example: Inverter (see lecture on digital electronics)



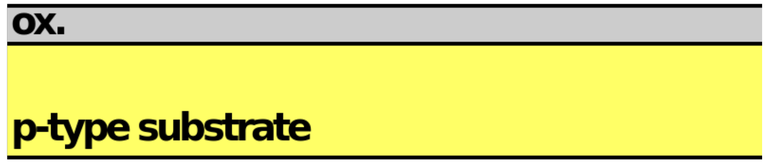
Main strengths:

- Low power: No current when state is not changed
- High robustness wrt noise / other disturbances

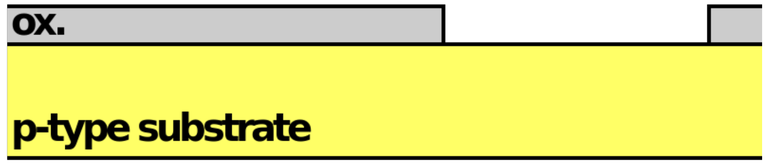
Also the production process is normally referred to as “CMOS”, not only the transistor concept.



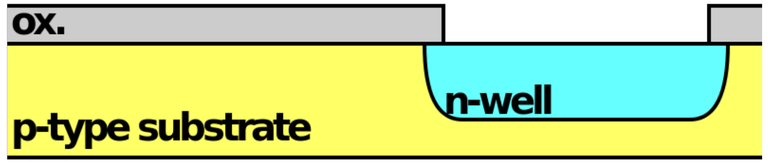
1. Grow field oxide



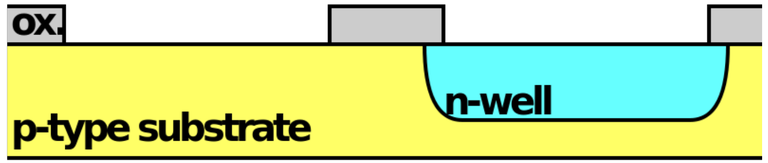
2. Etch oxide for pMOSFET



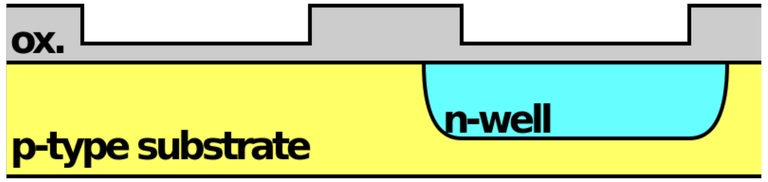
3. Diffuse n-well



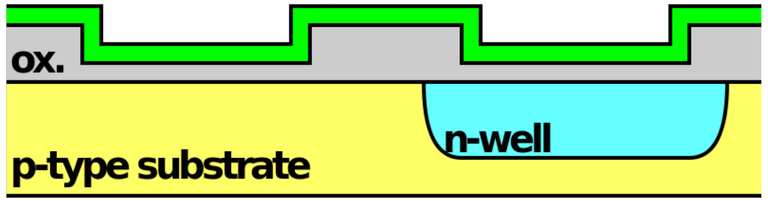
4. Etch oxide for nMOSFET



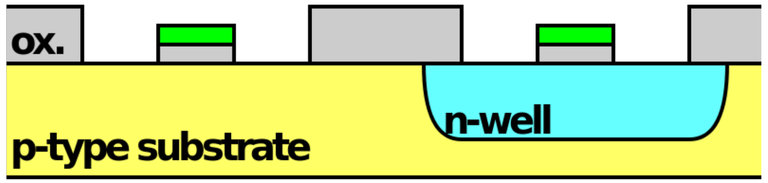
5. Grow gate oxide



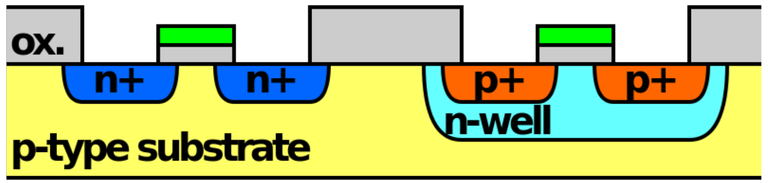
6. Deposit polysilicon



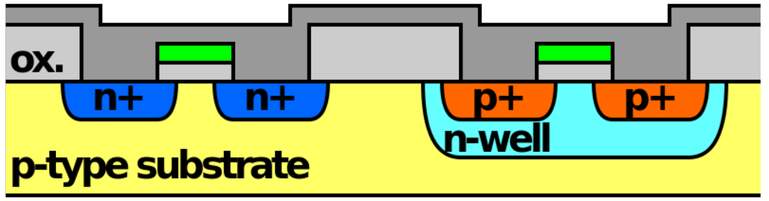
7. Etch polysilicon and oxide



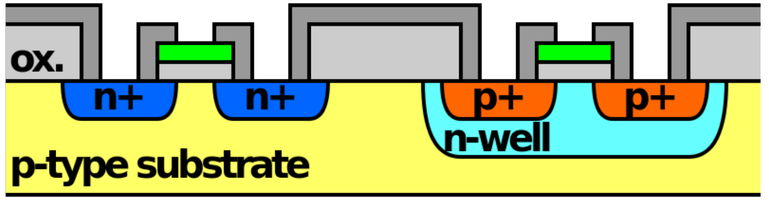
8. Implant sources and drains



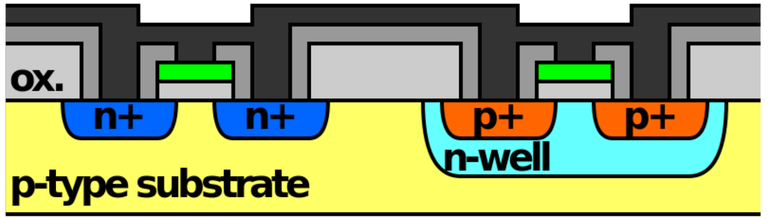
9. Grow nitride



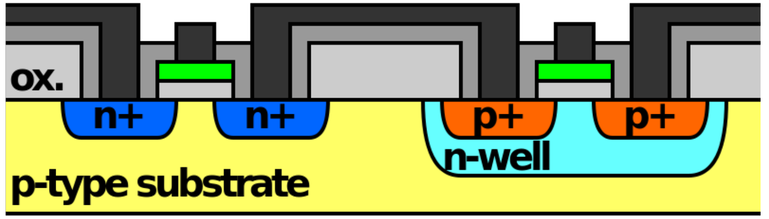
10. Etch nitride



11. Deposit metal



12. Etch metal



CMOS Technology Nodes

Technologieknoten

- Originally defined by the feature size: Half of the distance of the smallest elements (or of lines on the first “wiring level”). Given by the smallest structures that can be produced by photolithography in a given process.
  Now: Only an approximate relation - gate-length can be smaller or bigger. (-> Marketing term!)

Since ~ mid 1980ies: Standardization, now via “Technology Roadmaps”:

Stepts that double the density: Feature size per step1/√2 (~0.7)

Example: First roadmap of the Semiconductor Industry Association (SIA) 1993

Characteristic	1992	1995	1998	2001	2004	2007
Feature size (microns)	0.50	0.35	0.25	0,18	0,12	0.10
Gates per chip (millions)	0.3	0.8	2.0	5.0	10.0	20.0
Bits per chip						
DRAM	16M	64M	256M	1G	4G	16G
SRAM	4M	16M	64M	256M	1G	4G
Wafer processing cost ($/cm²)	$4.00	3.90	3.80	3.70	3.60	3.50
Chip size (mm²)						
logic	250	400	600	800	1,000	1,250
memory	132	200	320	500	700	1,000
Wafer diameter (mm)	200	200	200-400	200-400	200-400	200-400
Defect density (defects/cm²)	0.10	0.05	0.03	0.01	0.004	0.002
Levels of interconnect (for logic)	3	4-5	5	5-6	6	6-7
Maximum power (watts/die)						
high performance	10	15	30	40	40-120	40-200
portable	3	4	4	4	4	4
Power supply voltage						
desktop	5	3.3	2.2	2.2	1.5	1.5
portable	3.3	2.2	2.2	1.5	1.5	1.5

SIA 1993

CMOS Technology Nodes

A few Examples

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- 10 μm PMOS (1971): ex: Intel 4004; 190 transistors/cm^2
- 3 μm NMOS (1975): ex: Intel 8086; 880 transistors/cm^2
- 1 μm CMOS (1985): ex: Intel 80386; 7000 transistors/cm^2
- 0.35 μm (1995): ex: Intel Pentium 133; ~31k Tr/cm^2
- 180 nm (1999): ex: Intel Pentium III; 300k Tr/cm^2
- 65 nm (2006): ex: Intel Core 2; 2M Tr/cm^2
- 32 nm (2010): ex: Intel Westmere; 4.7M Tr/cm^2
- Intel 14 nm (2014): Broadwell; 16M Tr/cm^2
- TSMC N10 (2017): A10X; 34M Tr/cm^2
- Intel 10 nm (2018): Cannon Lake; 100M Tr/cm^2
- TSMC N5 (2020): Apple M1; 132M Tr/cm^2

Crucial technology: photolithography

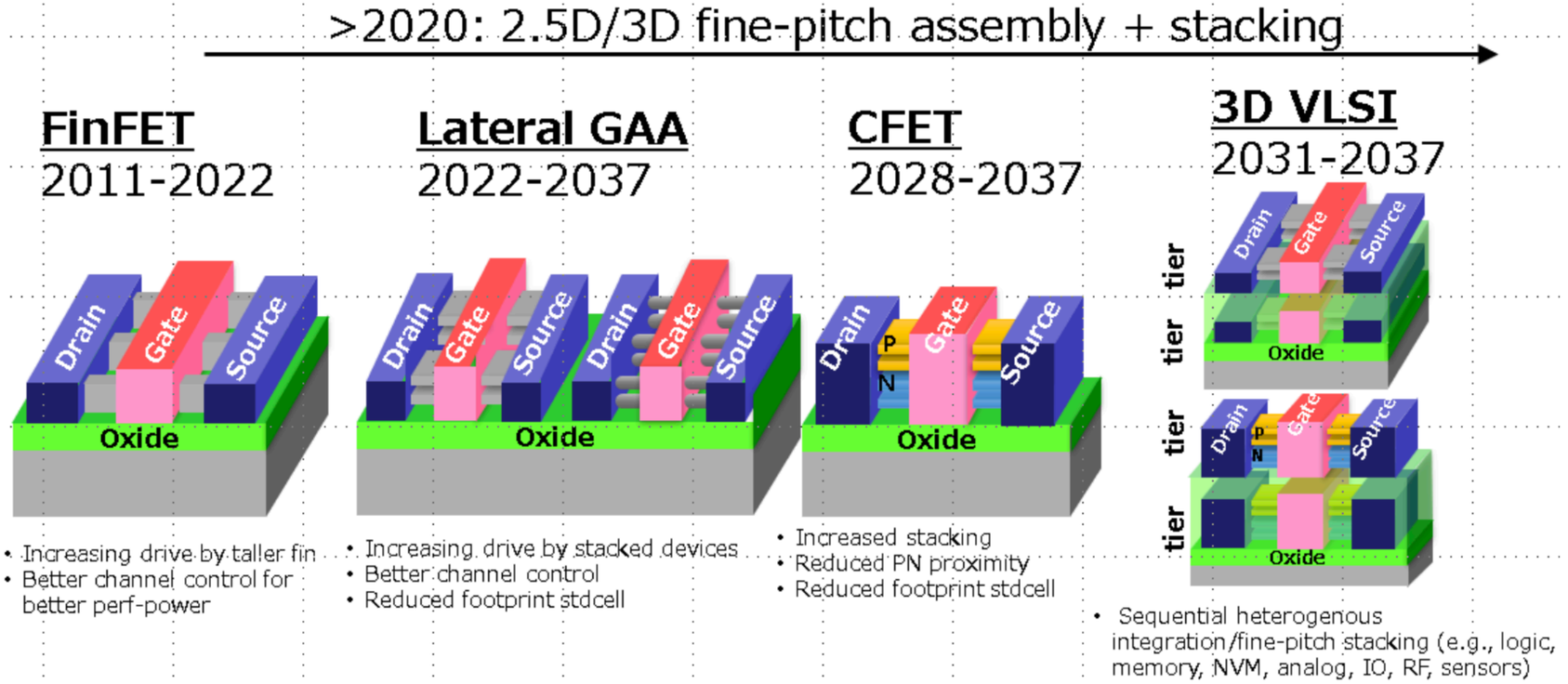
Wave length key for achievable feature size.

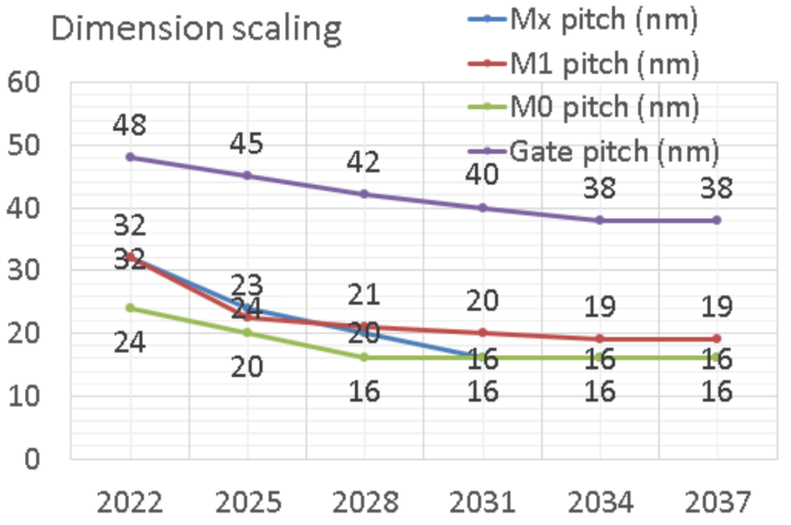
• 435 nm (Hg lamps)	
• 365 nm (Hg lamps)	ab 1985
• 248 nm KrF excimer laser	ab 1999
• 193 nm ArF excimer laser	ab 2004
• 13.5 nm EUV	ab 2019

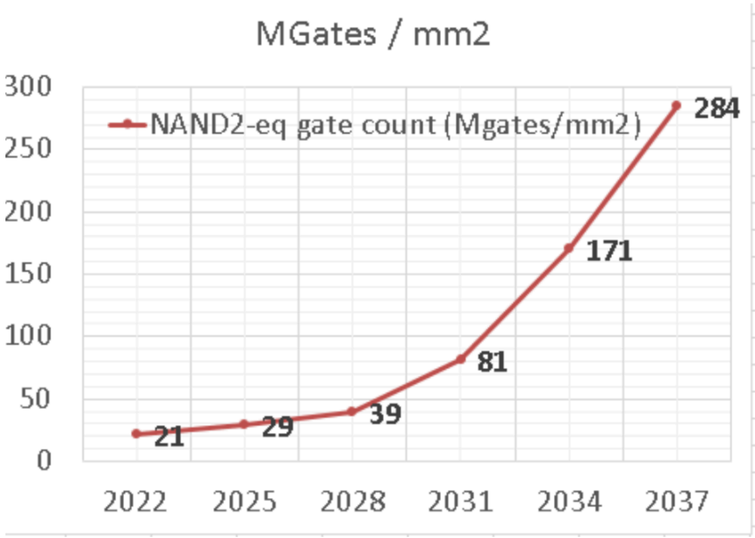
Below 65 nm: Improvements not only driven by feature size, but also by new design of transistors, for example high-k dielectrics, FinFETs, multi-gate, gate-all-around,…

Weitere Entwicklung

Moore am Laufen halten



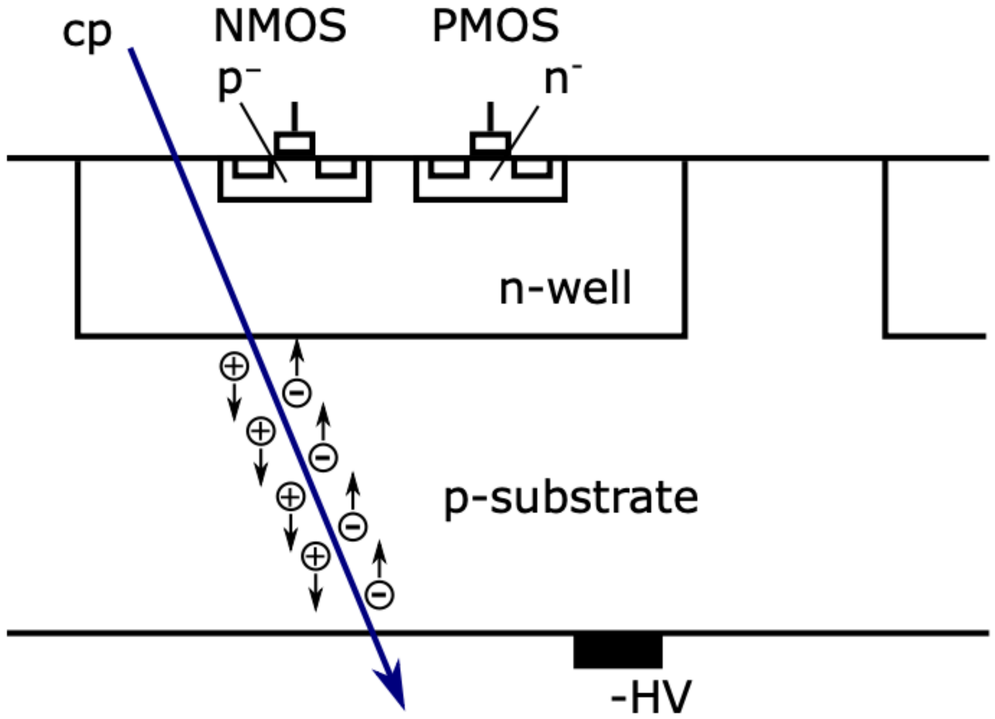




CMOS Technology for Detectors

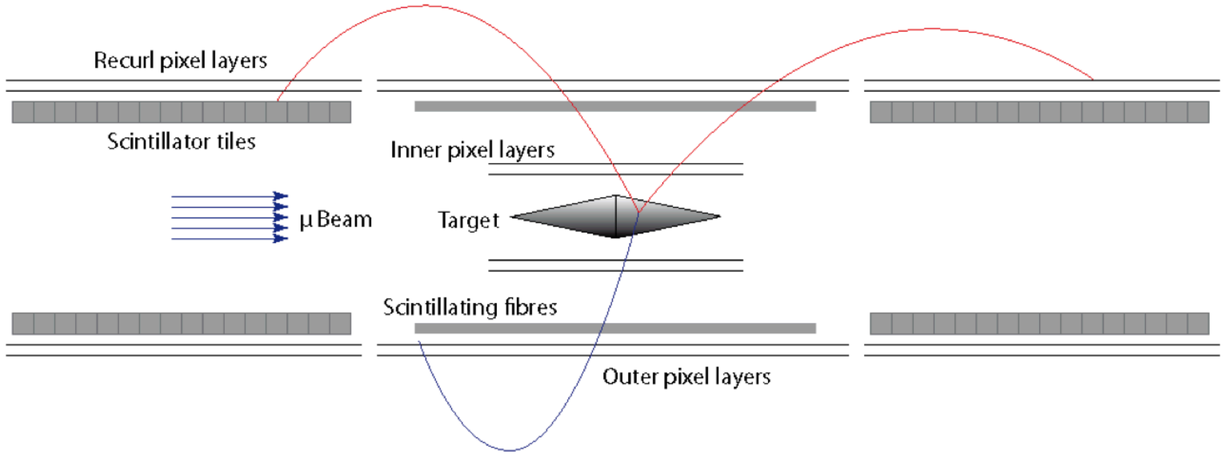
Examples from High Energy Physics

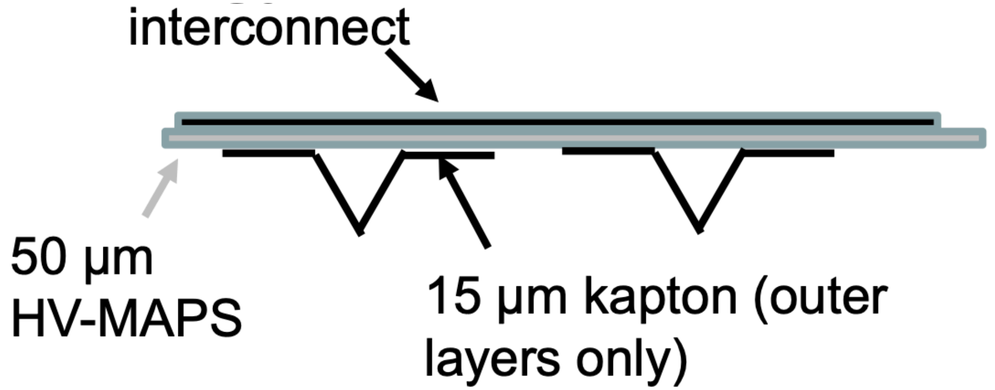
- “Monolithic active pixel sensor” MAPS



MSc thesis Felix Ehrler, IPE (2015)

HVCMOS technology: Ivan Peric, IPE





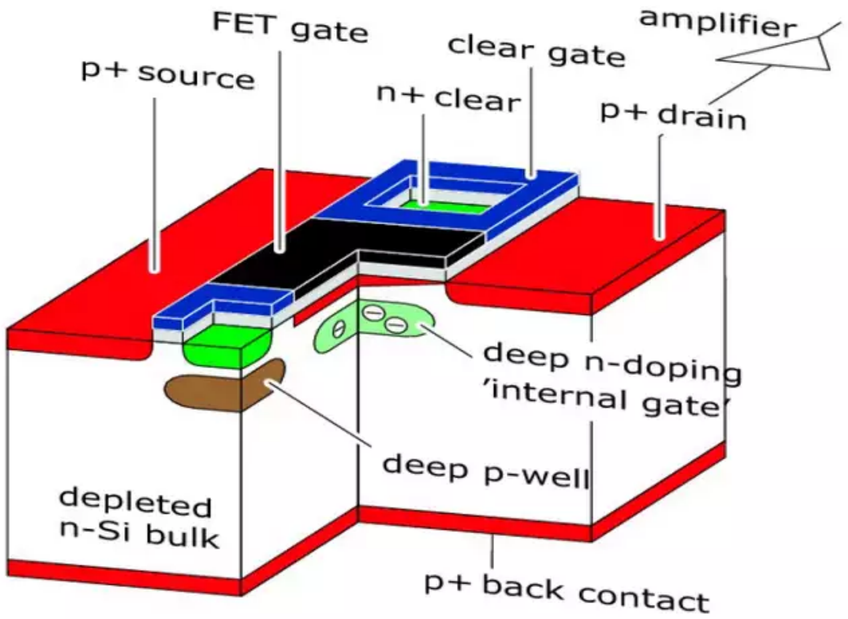
Mu3e experiment

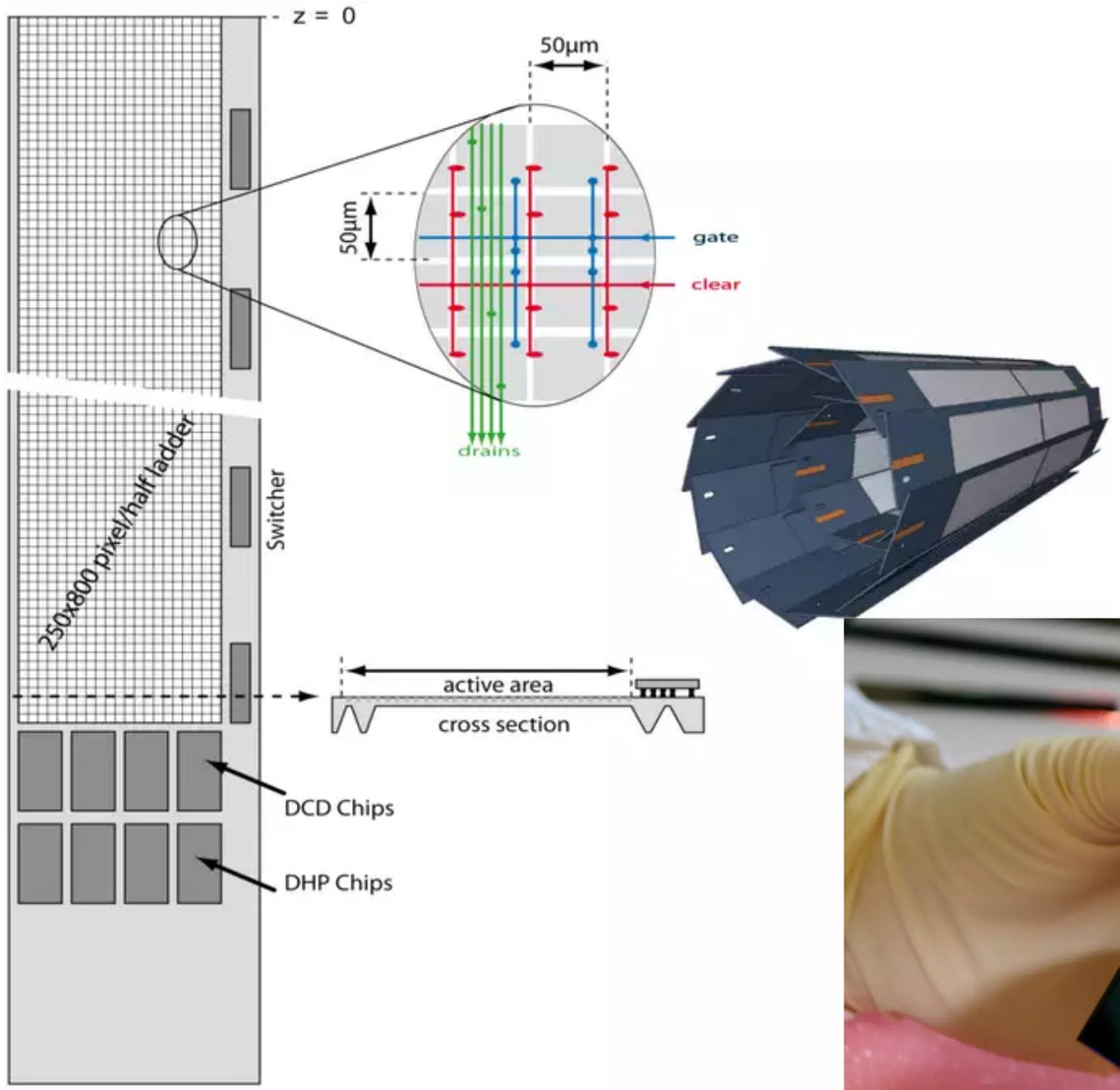
Technologie also in discussion for LHCb Upgrade II

CMOS Technology for Detectors

Examples from High Energy Physics

- “Monolithic active pixel sensor” MAPS





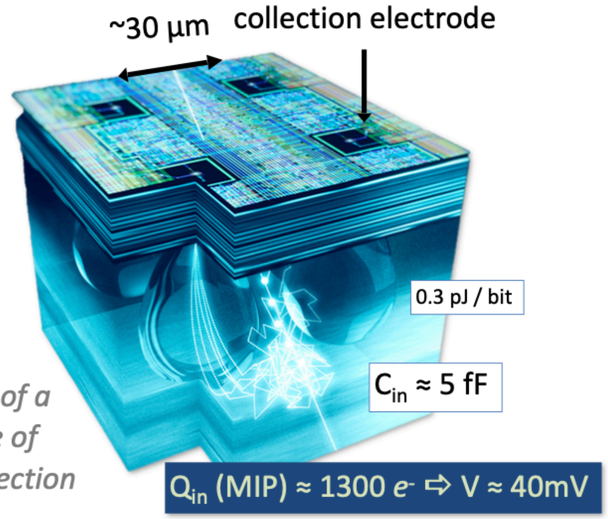
DEPFET, MPG HLL

Belle II PXD

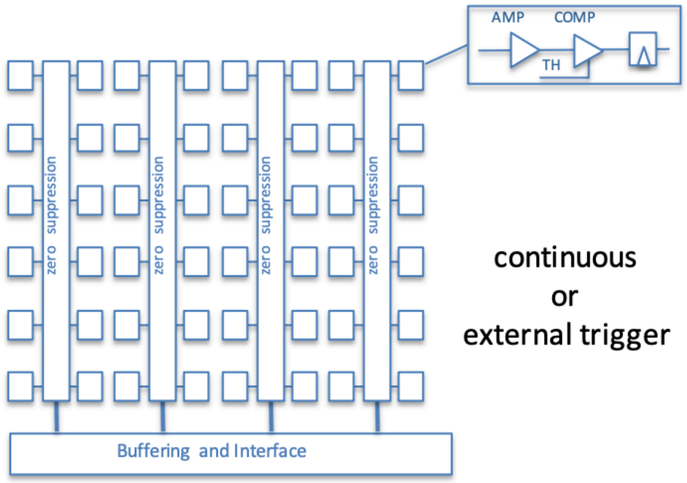
Addt’l ASICs: IPE

ALPIDE — the Monolithic Active Pixel Sensor (MAPS) for ITS2

ALICE



Artistic view of a SEM picture of ALPIDE cross section



continuous or external trigger

- Developed within the ITS2 project

Technology

Technology now used in other applications

- TowerJazz 180 nm CMOS Imaging Process
- High-resistivity (> 1kΩ cm) p-type epitaxial layer (25 µm) on p-type substrate
- Small n-well diode (2 µm diameter), ~100 times smaller than pixel (~30 µm)
  ➔ low capacitance (~fF)
- Reverse bias voltage (-6 V < V_{BB} < 0 V) to substrate to increase depletion zone around NWELL collection diode
- Deep PWELL shields NWELL of PMOS transistors
  ➔ full CMOS circuitry within active area

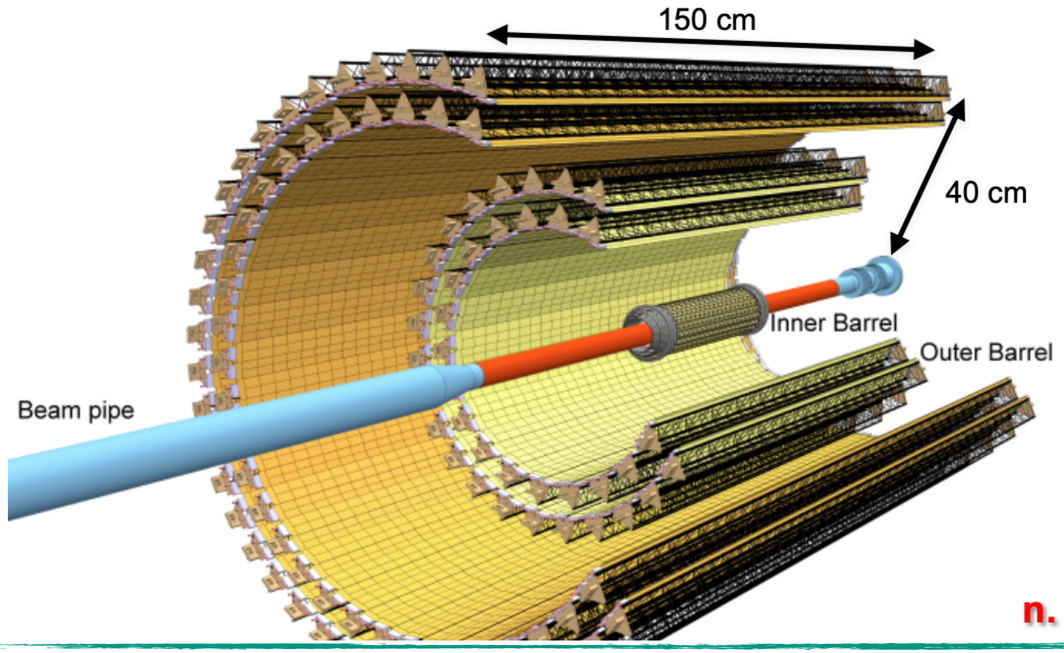
Key features

- In-pixel amplification and shaping, discrimination and Multiple-Event Buffers (MEB)
- In-matrix data sparsification
- On-chip high-speed link (1.2 Gbps)
- Low total power consumption < 40 mW/cm²

ITS2 layout

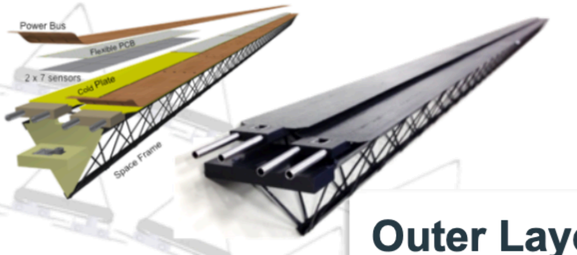
- 7 layers (inner/middle/outer): 3/2/2 from R = 23 mm to R = 400 mm
- 192 staves (IL/ML/OL): 48/54/90
- Ultra-lightweight support structure and cooling

10 m² active silicon area, 12.5×10⁹ pixels



ALICE

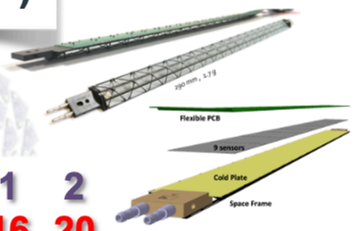
Outer Barrel (OB) = ML + OL



Outer Layers (OL)

Middle Layers (ML)

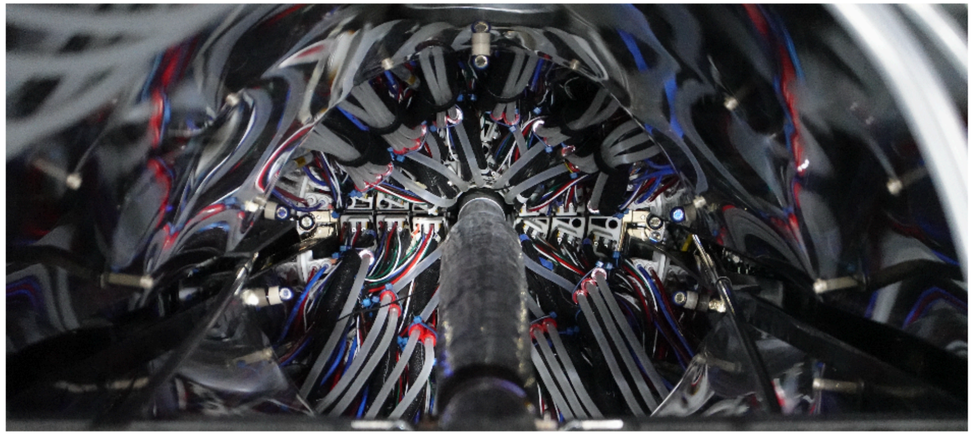
Inner Barrel (IB)



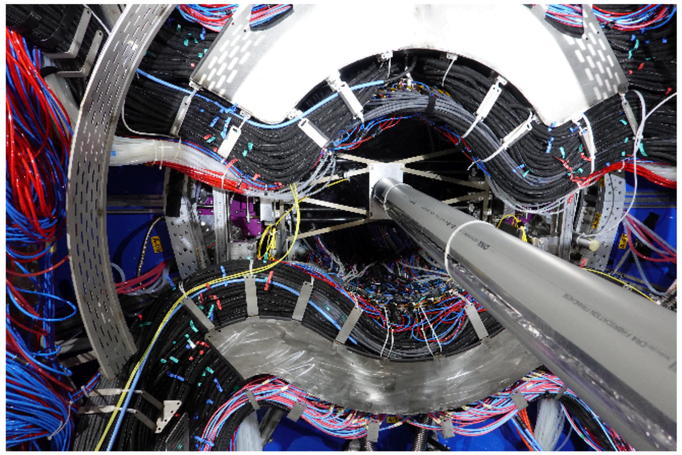
Layer #	0	1	2	3	4	5	6
n. of Staves	12	16	20	24	30	42	48

ITS2 in the ALICE experimental apparatus now

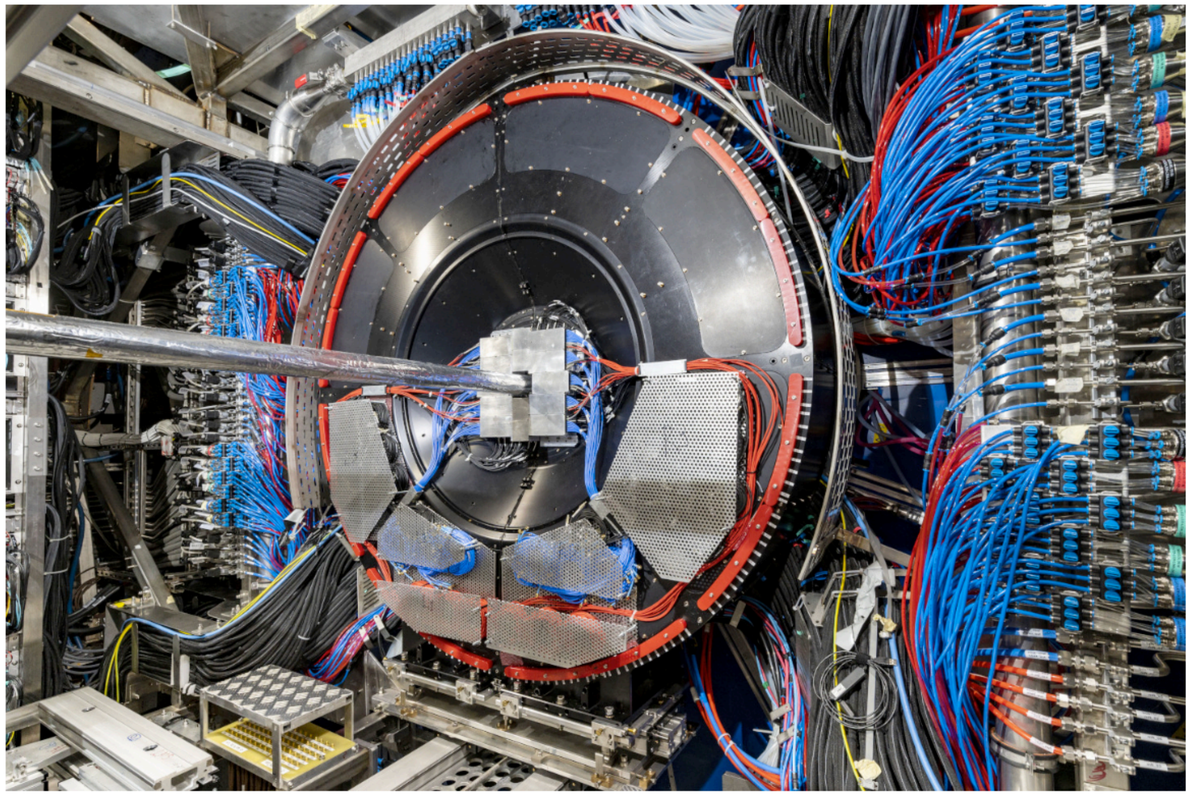
ALICE



Inner Barrel fully mated - only services visible



Full services connected (data, power, cooling, ventilation)



Fast Interaction Trigger (FIT) installed in from of the ITS and its services

CMOS Technology for Detectors

Examples from High Energy Physics

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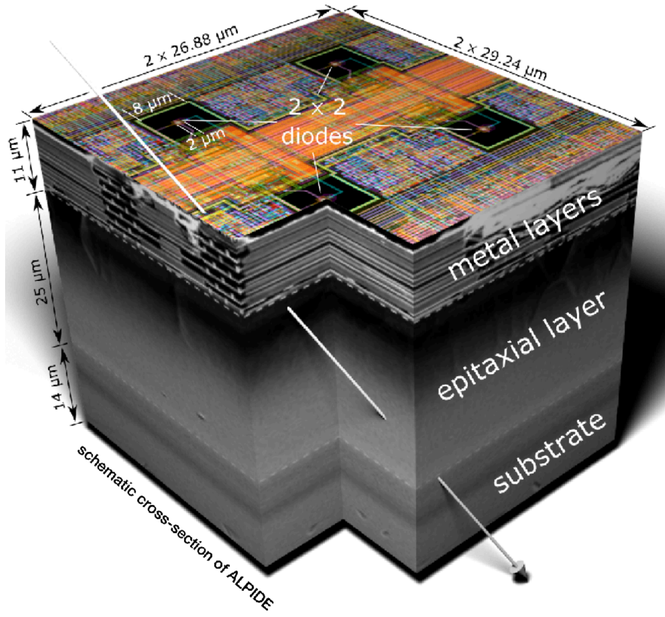
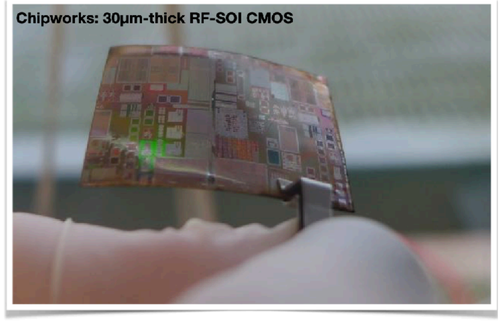
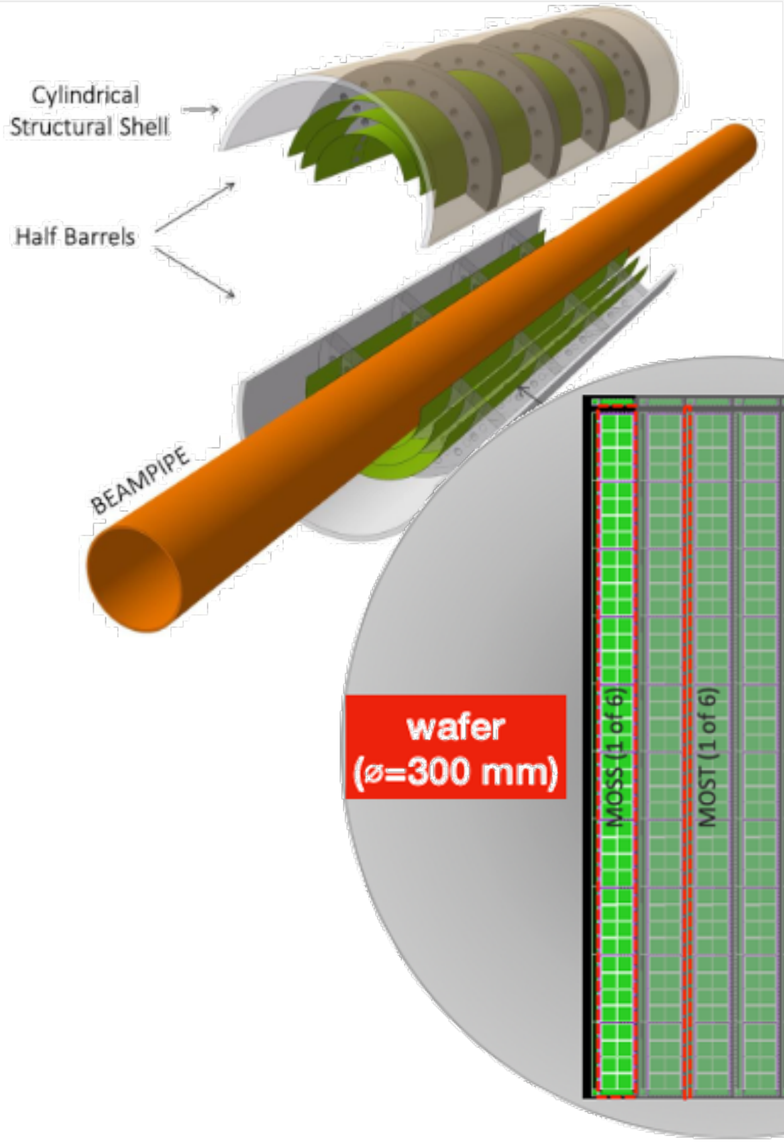
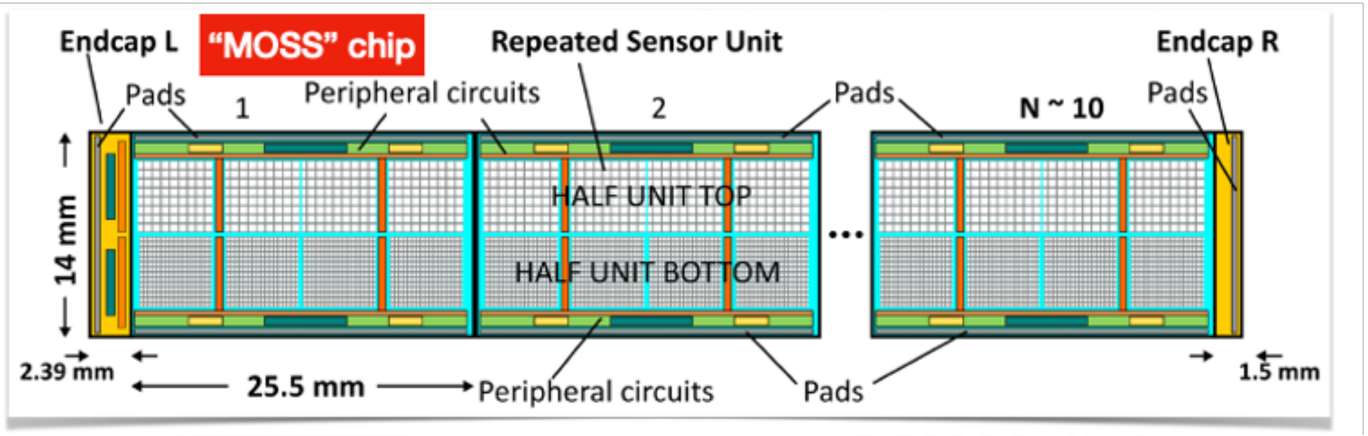
ALICE ITS3







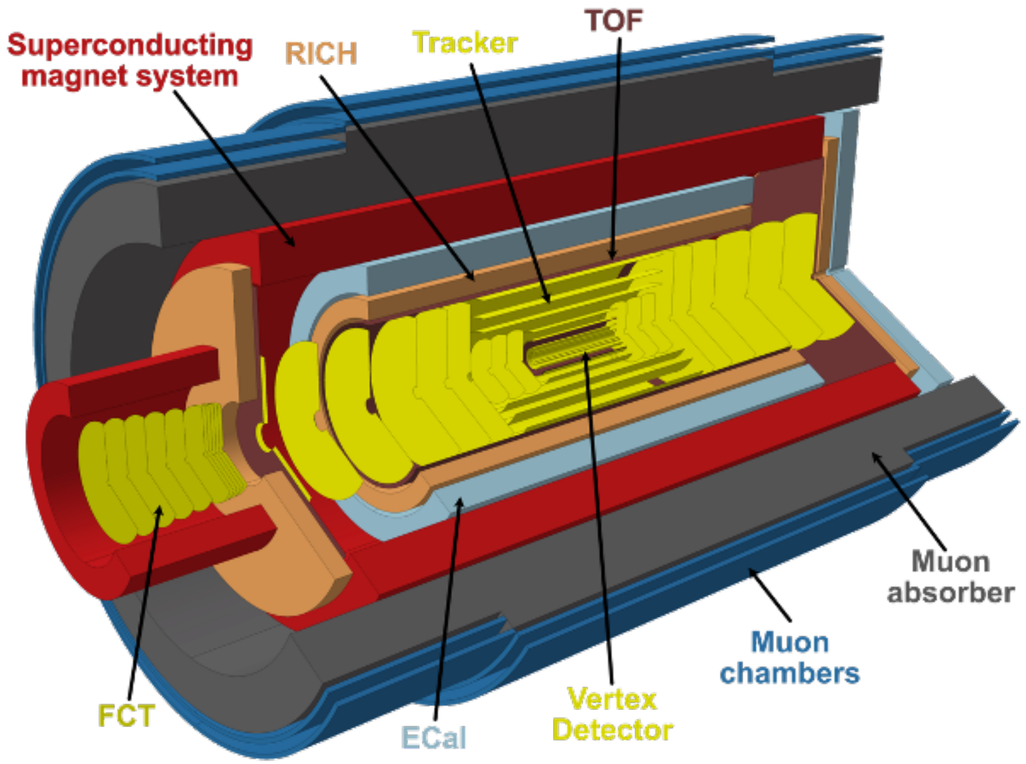


CMOS Technology for Detectors

Examples from High Energy Physics: Ambitious Plans

- Phase IIb Upgrades am LHC: Entwicklung jetzt, konkretes technisches Design ~ 2026, Einbau ~ 2033

ALICE 3

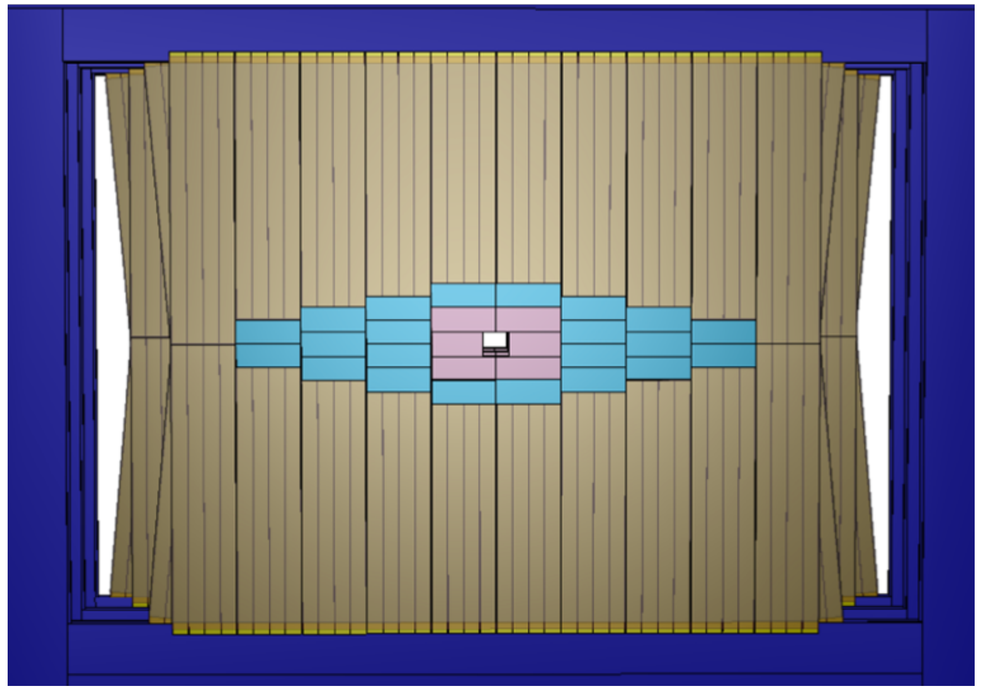


~ 60 m² CMOS sensor tracker

~ 45 m² CMOS timing sensors

Light sensors for RICH (~ 35 m², two layers: sensor, RO)

LHCb Upgrade II



"Mighty tracker": HV-CMOS + Scintillating fibers (~ 15 m² CMOS area)

+ 4D-Tracking (VELO, UT)

CMOS Technology for Detectors

Examples from High Energy Physics: And even more ambituous Dreams

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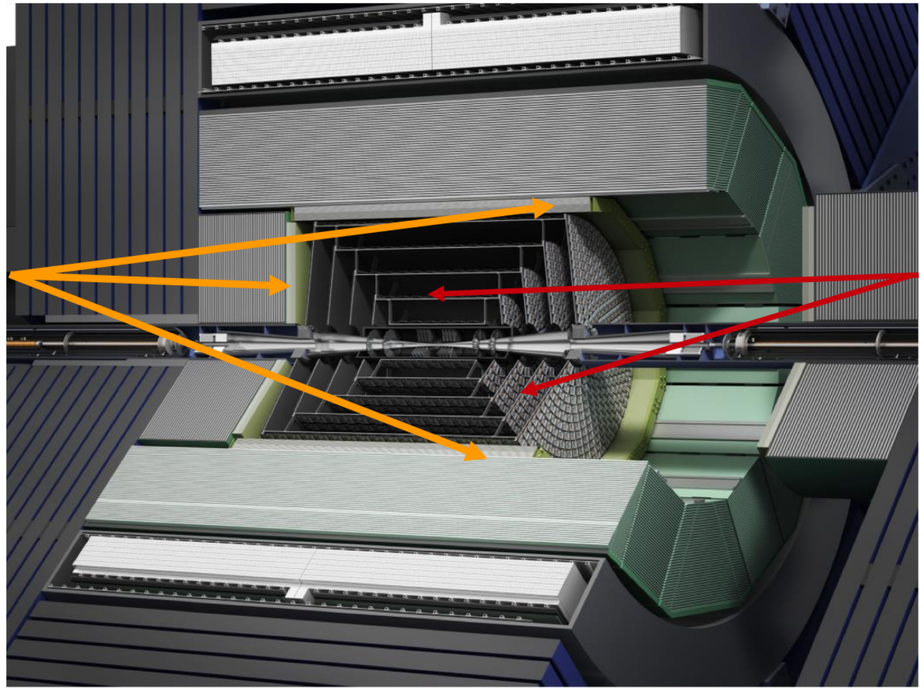
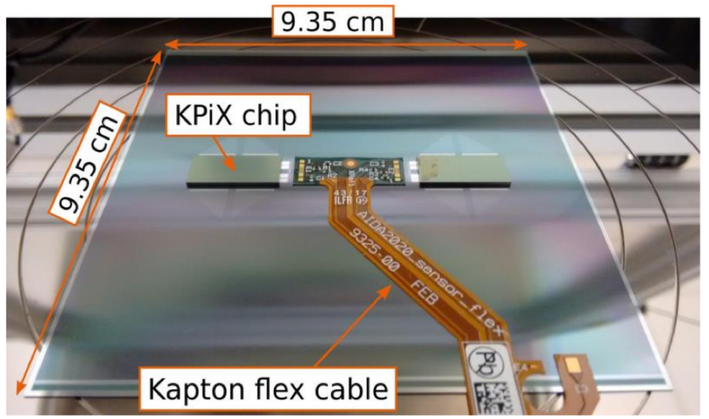
- For a future Higgs Factory (operation mid 2040ies or later): Several detector concepts with CMOS-based silicon tracking, and silicon-based electromagnetic calorimetry.
- One example: the SiD detector concept -> All-CMOS out to the ECAL.

ECAL:
1200 m^2 sensor area





Tracker:
67 m^2 sensor area

NB: Currently simulation studies, backed up by small-size component demonstrators - still a long (and very uncertain) way to realization!

Next Lectures:

Digital - Thursday, February 1

Analog 13 - Chapter 07 - Tuesday, February 6, 2024

Time Plan for Next Lectures

A few Changes coming up!

Calender Week	Tuesday	Thursday
45	07.11. **Analog**	09.11. **Digital**
46	14.11. **Analog**	16.11. **Digital**
47	21.11. **Digital**	23.11. **Analog**
48	28.11. **Digital**	30.11. **Digital**
49	05.12. **Digital**	07.12. **Analog**
50	12.12. **Digital**	14.12. **Analog**
51	19.12. **Analog**	21.12. **Digital**
2	09.01. **Analog**	11.01. **Digital**
3	16.01. **Digital**	18.01. **Digital**
4	23.01. **Analog**	25.01. **Digital**
5	30.01. **Analog**	01.02. **Digital**
6	06.02. **Analog**	08.02. **Analog**
7	13.02. **Analog**	15.02. **Digital**

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KIT, Winter 2023/24

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