

Electronics for Physicists

Analog Electronics

Chapter 7; Lecture 13

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Chapter 7

Field Effect Transistors

- MOSFET Basics
- Excursion: CMOS Technology
- CMOS Circuits

Overview

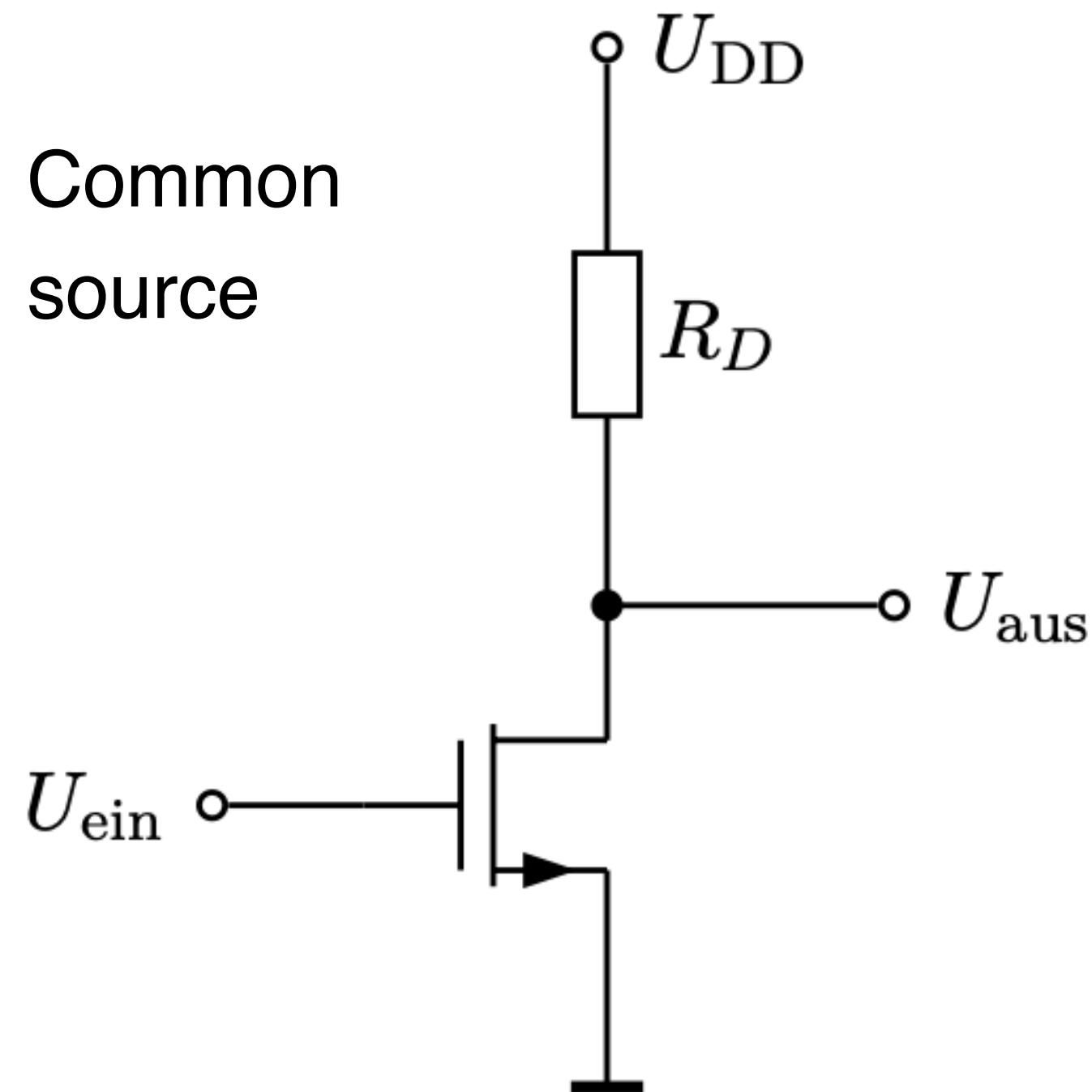
1. Basics
2. Circuits with R, C, L with Alternating Current
3. Diodes
4. Operational Amplifiers
5. Transistors - Basics
6. 2-Transistor Circuits
- 7. Field Effect Transistors**
8. Additional Topics
 - Filters
 - Voltage Regulators
 - Noise

CMOS Circuits - Cont'd

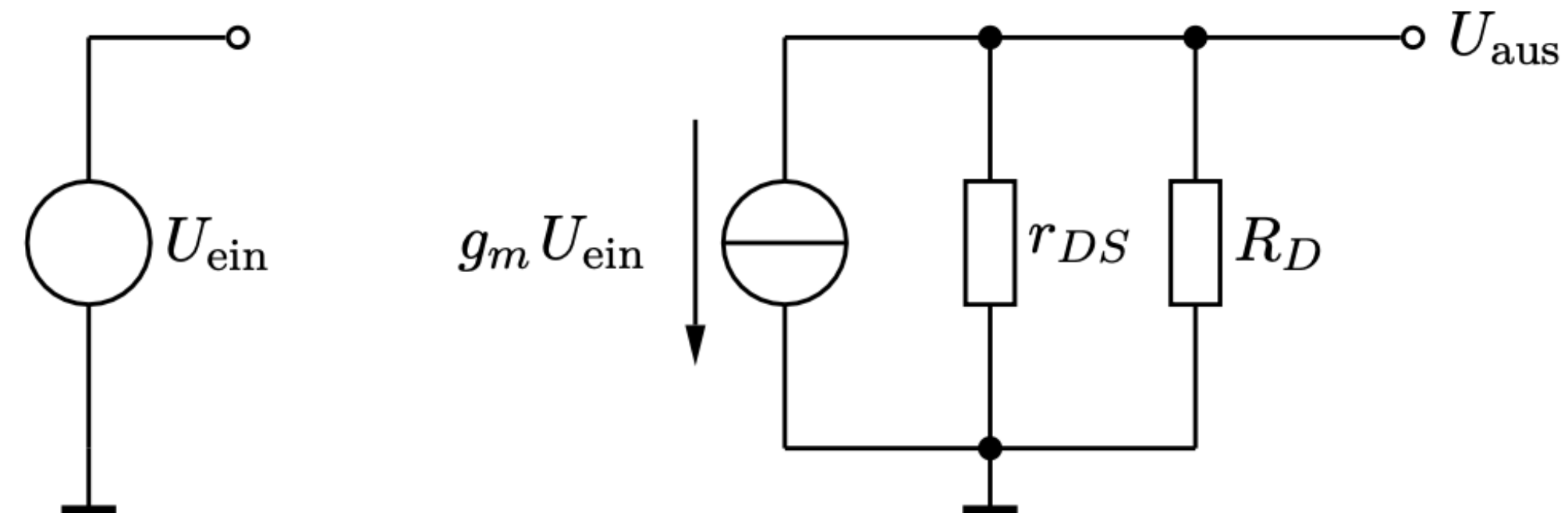
In: Chapter 7: Field Effect Transistors

Common Source Amplifier

The Equivalent to the Common Emitter



- Small signal replacement circuit:



Amplification:

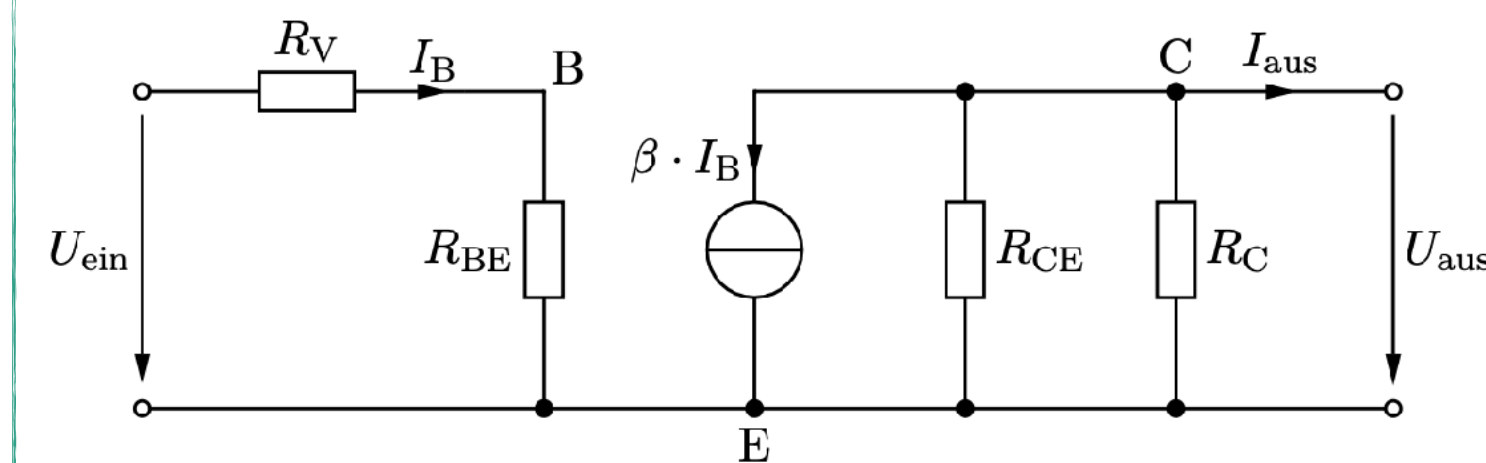
$$V_U = \frac{dU_{aus}}{dU_{ein}} = - \frac{(r_{DS} \parallel R_D) g_m dU_{ein}}{dU_{ein}} = - (r_{DS} \parallel R_D) g_m \approx -g_m R_D \quad (R_D \ll r_{DS})$$

Impedances:

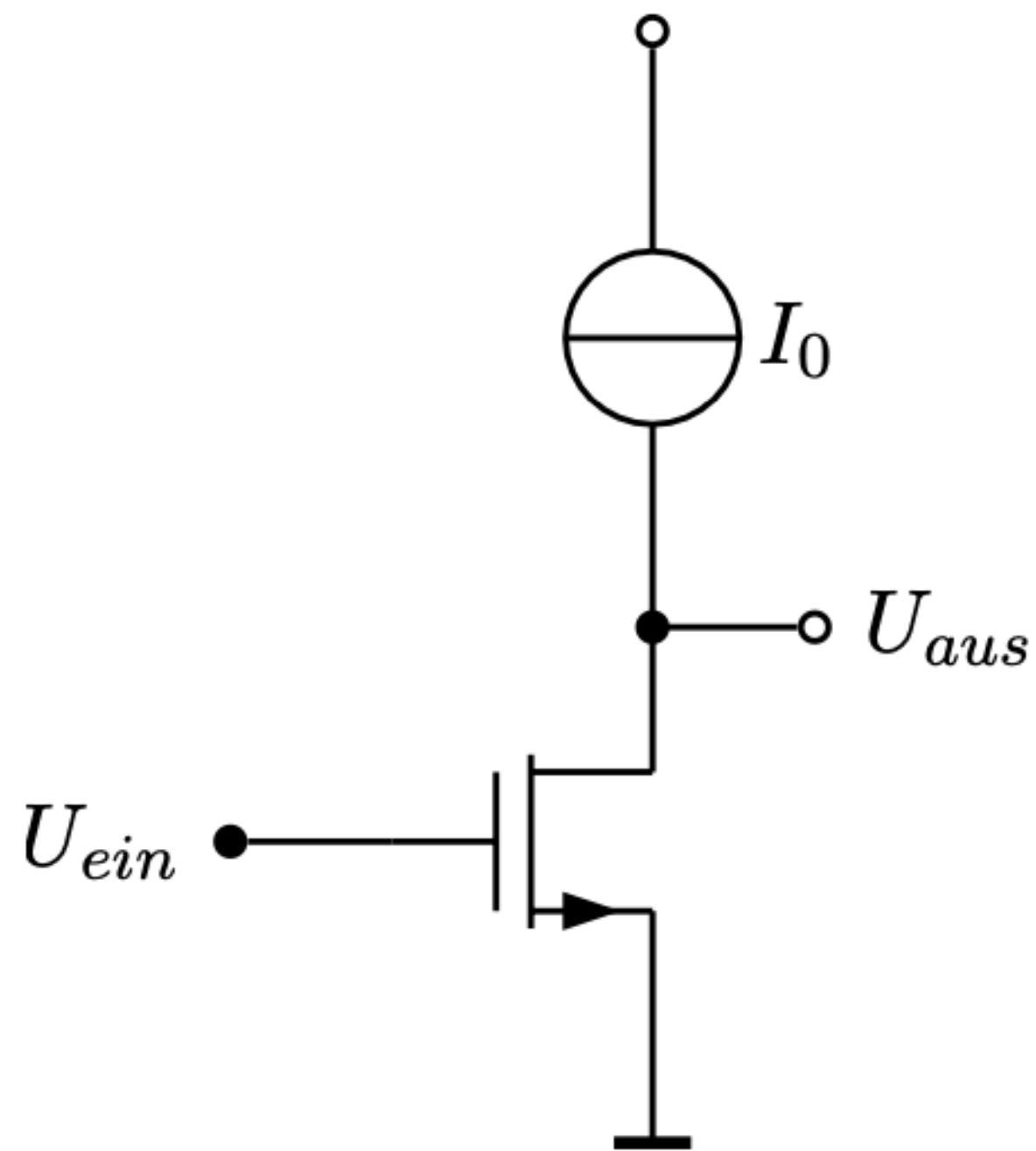
$$R_{ein} = \frac{dU_{ein}}{dI_{ein}} \approx \infty$$

$$R_{aus} = \frac{dU_{aus}}{dI_{aus}} = R_D \parallel r_{DS} \approx R_D$$

Reminder: BJT common emitter



- Replacing R_D with a current source:



Amplification depends R_D : Large internal resistance = large amplification

Technical aspect: large resistors need lots of space in CMOS technology

Amplification here: $V_U = -g_m (r_{DS} \parallel R_i) \approx -g_m r_{DS} = -\frac{g_m}{g_{DS}}$ ($R_i \gg r_{DS}$)

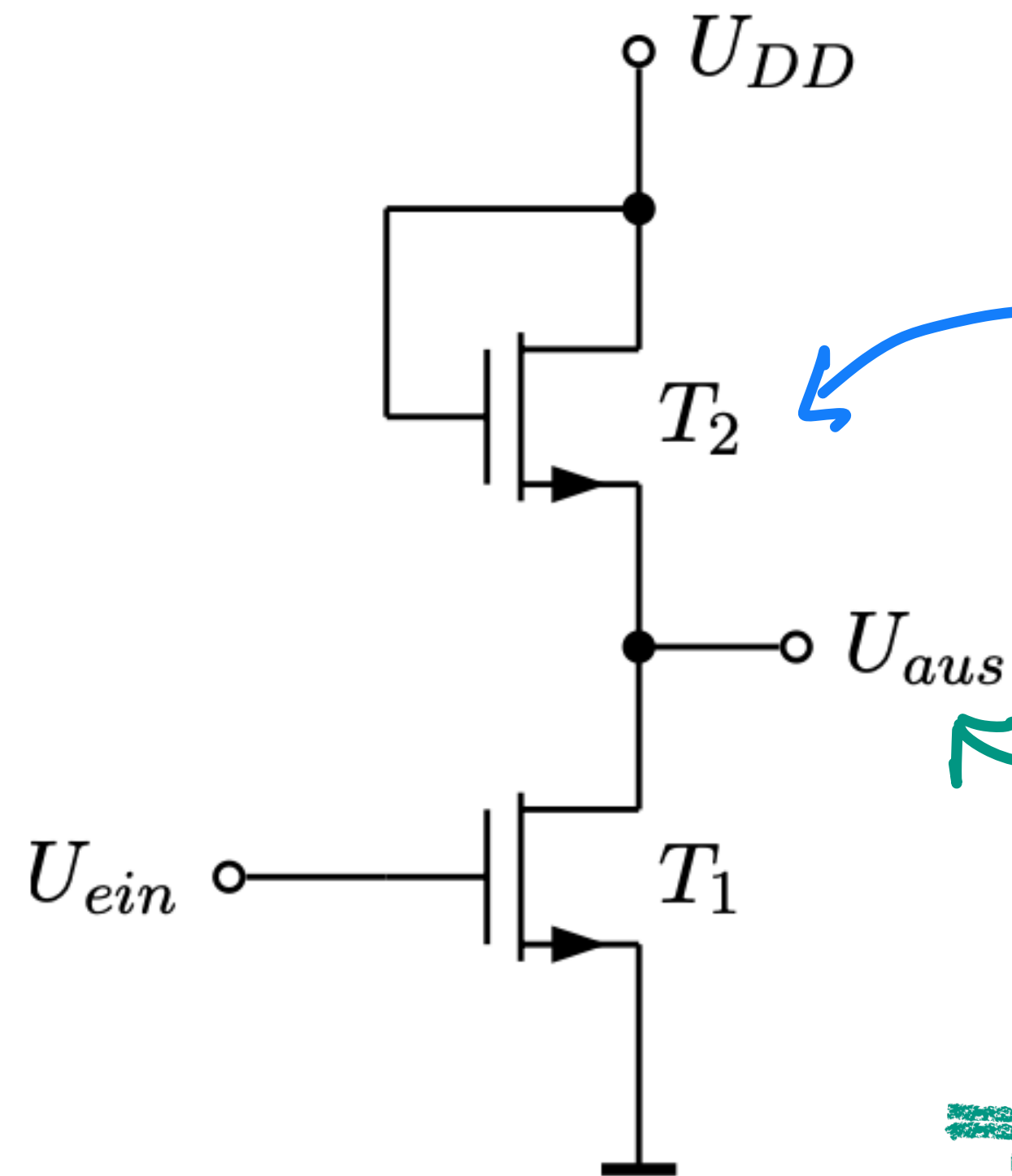
Numerical example:

$I_{DS} = 100 \mu A$; $\lambda \approx 0.1 \text{ V}^{-1} \Rightarrow g_{DS} \approx \lambda I_{DS} = 10 \mu S$

Für $g_m \approx 100 \mu S$: $V_U \approx 10$

Common Source Amplifier

Concrete Implementation: FET Diode as Current Source



• In this configuration:

$$r_{DS,2} = \frac{1}{g_{m,2}} \quad (\text{see S. 17})$$

$\Rightarrow$ amplification!

$$V_u = -g_{m,1} r_{DS,2} = -\frac{g_{m,1}}{g_{m,2}}$$

$$\Rightarrow V_u = -\sqrt{\frac{\left(\frac{W}{L}\right)_1}{\left(\frac{W}{L}\right)_2}}$$

$\Rightarrow T_1$ geometrically very large.
High amplification
impossible!

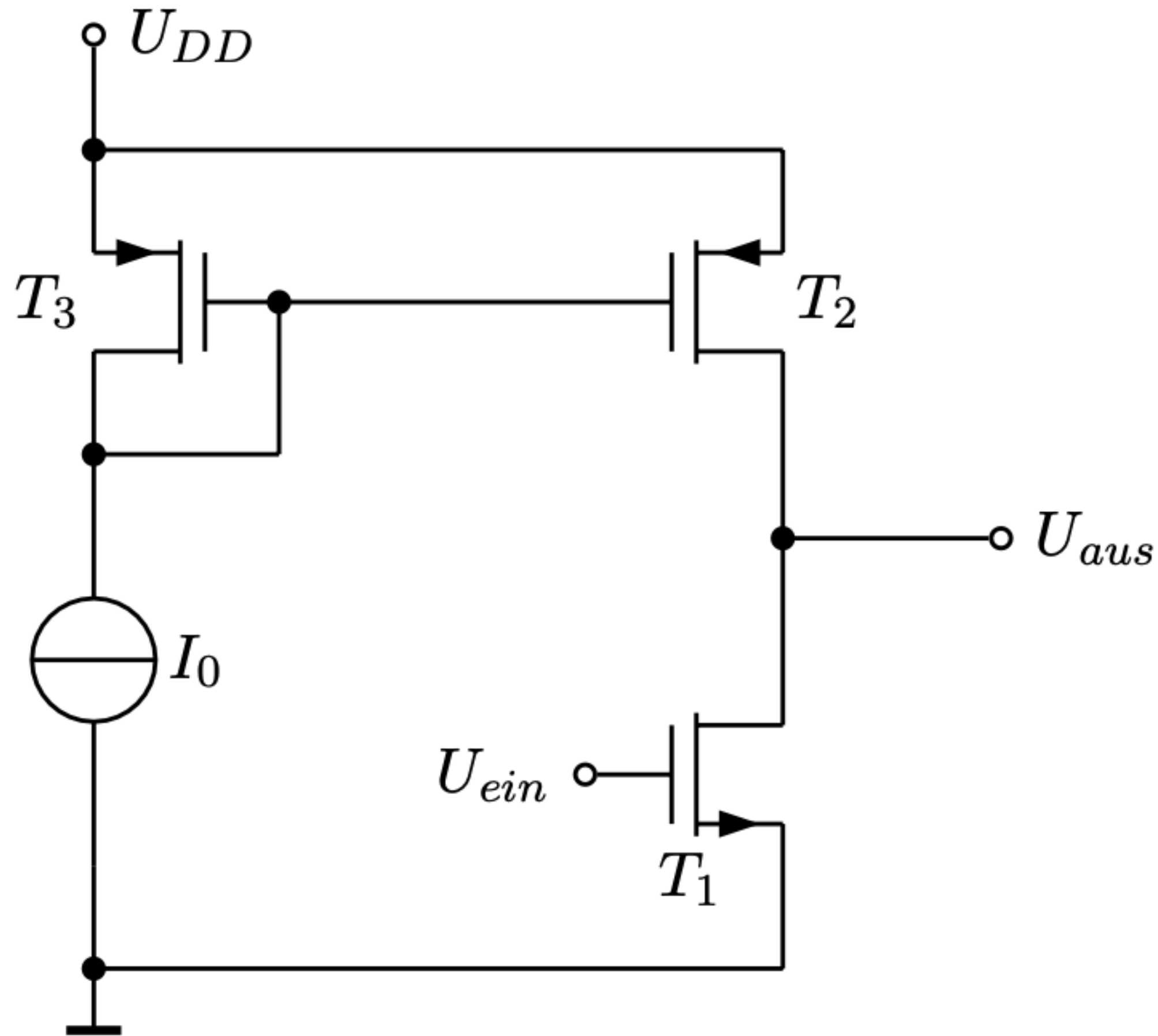
In the saturation region:

$$g_m = \sqrt{2\beta I_{DS}}$$

$$\beta = \mu C_{ox} \frac{W}{L}$$

Common Source Amplifier

More “Bang”: Current Mirror as Current Source



In contrast to FET diode: Feedback and current into amplifier separated, with that:

Differential source-drain resistance not determined by amplification, but by R_{DS} .

Amplification:

$$V_U = -g_{m1} (r_{DS1} \parallel r_{DS2}) \quad \text{here: } r_{DS2} \gg 1/g_{m2}$$

Accurate for small currents I_{DS} , since $r_{DS} = 1/g_{DS}$; $g_{DS} \approx \lambda I_{DS}$

Numerical example:

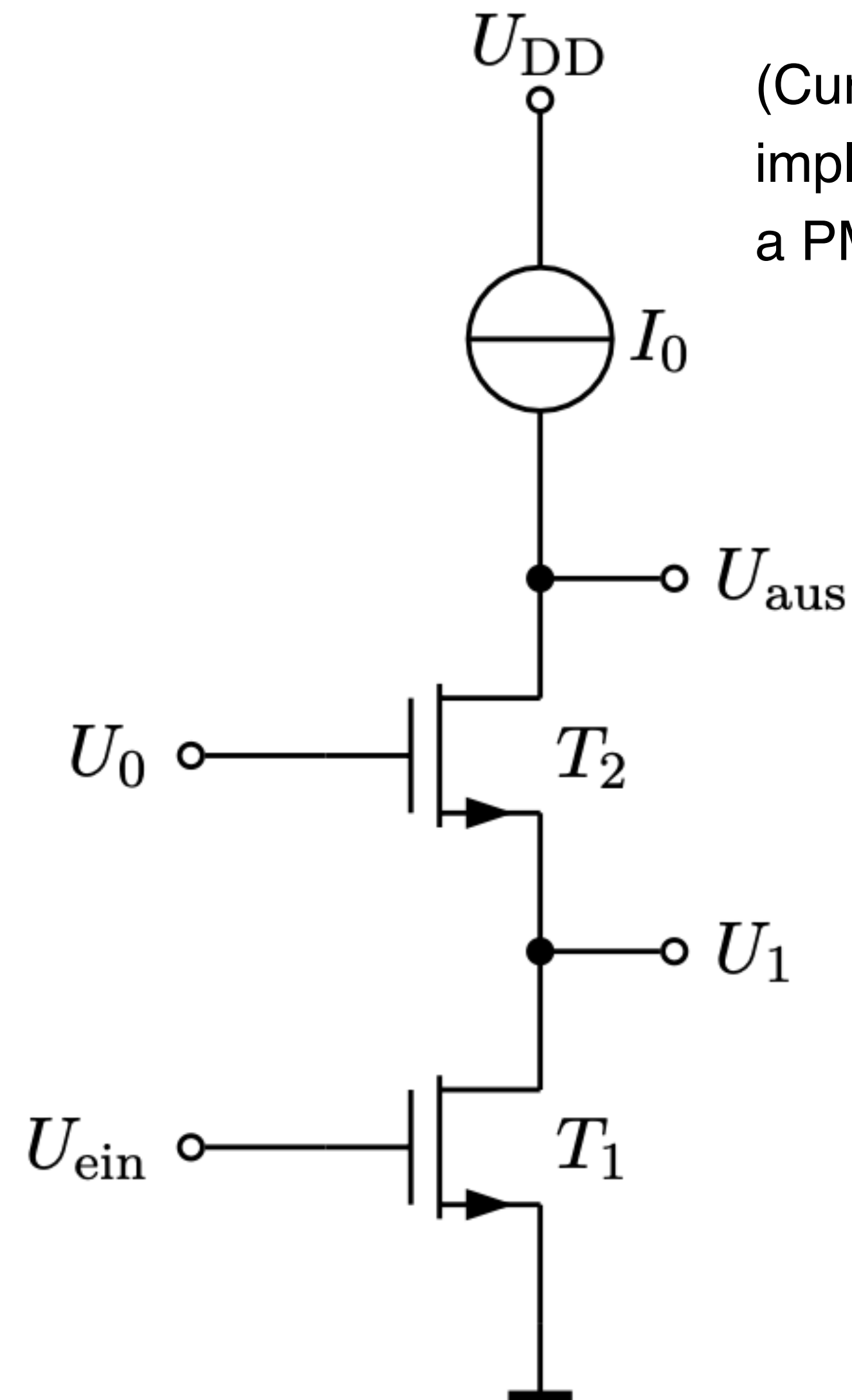
$$g_m \approx 100 \mu S; I_{DS} \sim 10 \mu A$$

$$\text{mit } \lambda \approx 0.1 \text{ V}^{-1} \Rightarrow g_{DS} \approx \lambda I_{DS} = 1 \mu S \Rightarrow r_{DS} = 1 \text{ M}\Omega$$

$$\Rightarrow V_U = -50$$

Cascode

The Path to larger Amplification



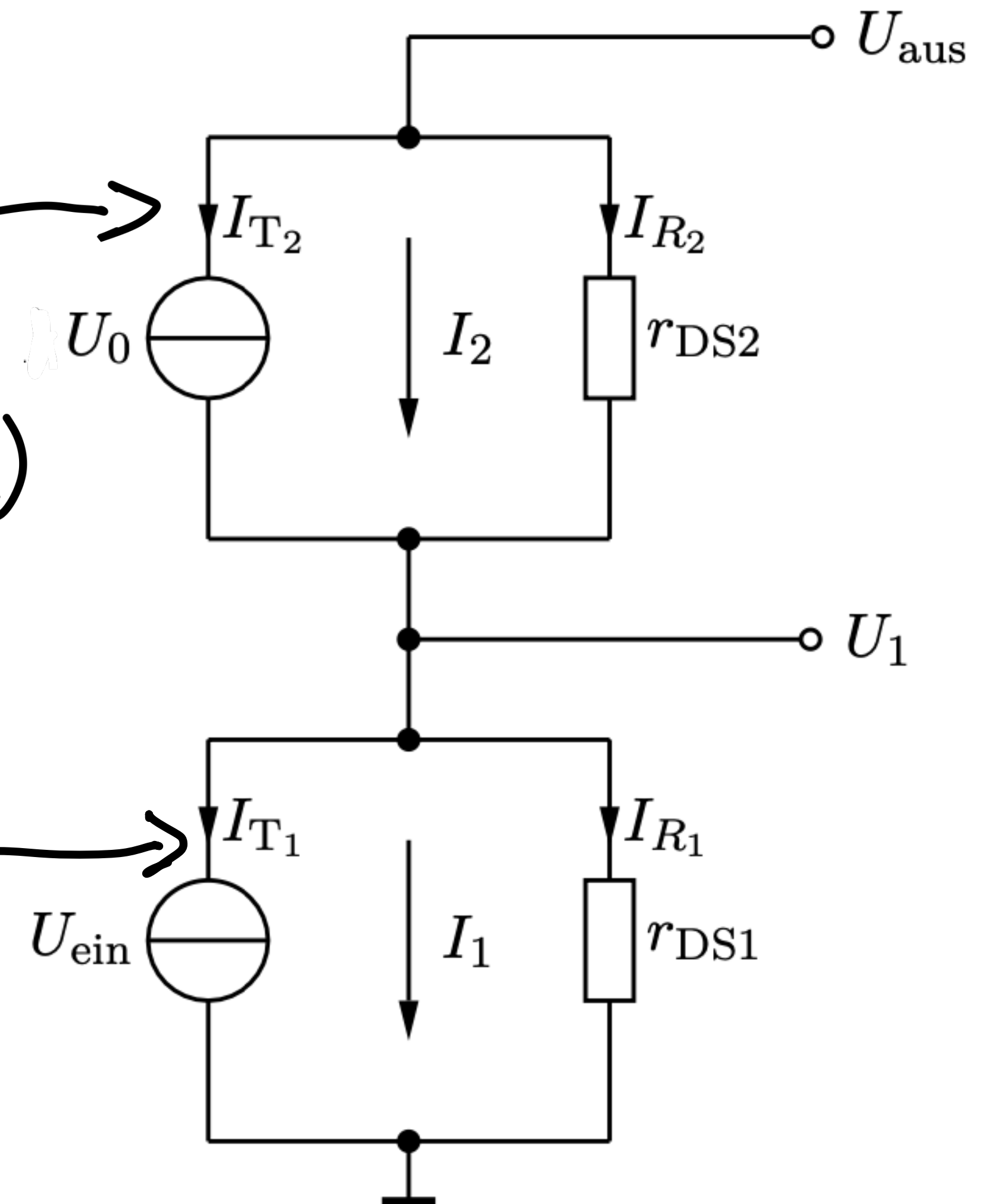
with:

$$g_m = \frac{dI_{DS}}{dU_{GS}}$$

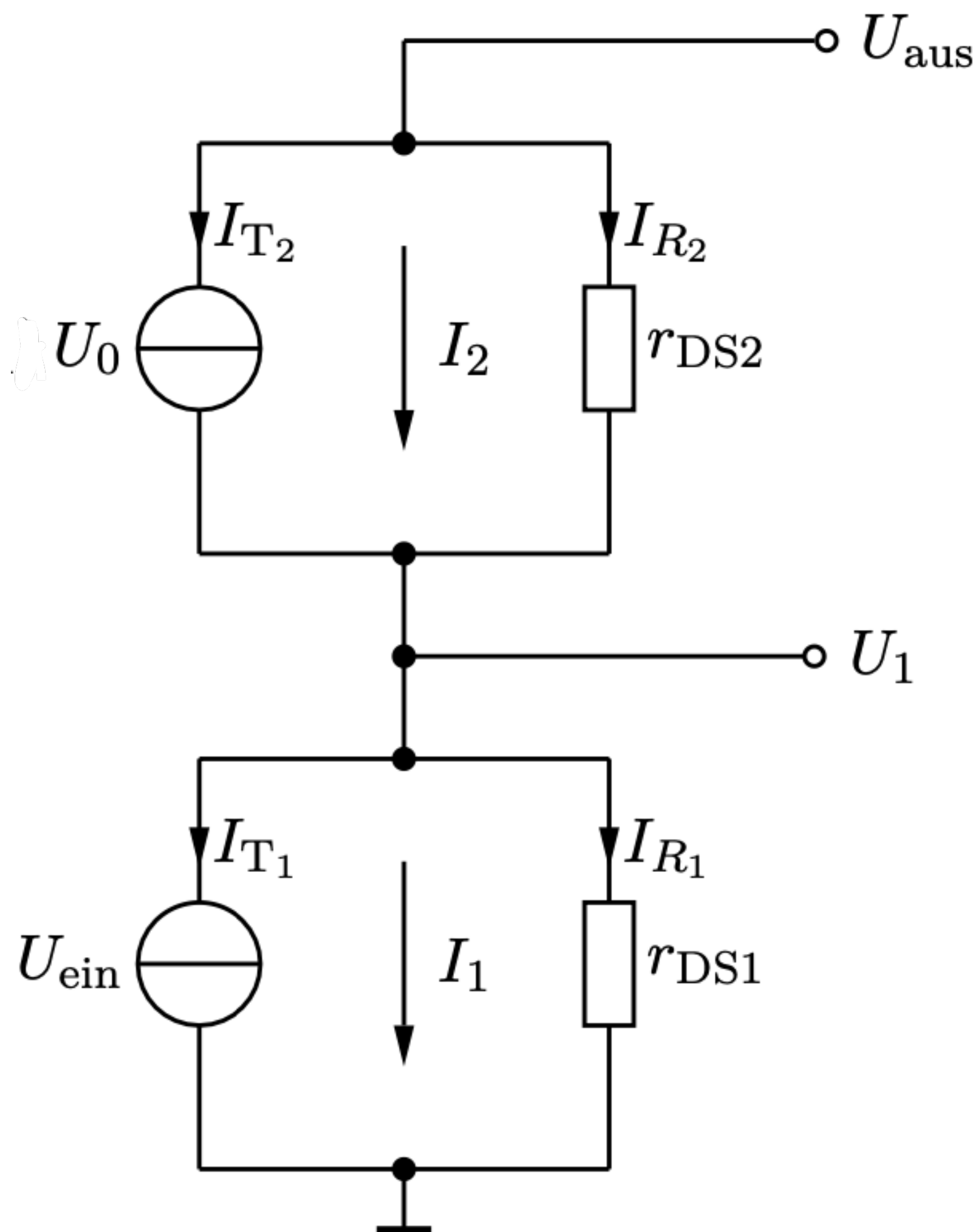
$$I_{T2} = g_{m2} (U_0 - U_1)$$

$$I_{T1} = g_{m1} U_{ein}$$

Small signal replacement circuit



- How it works:



Current source I_0 (not shown in small signal replacement circuit) defines the current in the circuit. With that:

$$dI_1 = g_{m1} dU_{ein} + \frac{dU_1}{r_{DS1}} = 0$$

$$\Rightarrow dU_1 = -g_{m1} dU_{ein} \cdot r_{DS1}$$

$$dI_2 = g_{m2} (dU_0 - dU_1) + \frac{dU_{aus} - dU_1}{r_{DS2}} = 0$$

(ext. voltage)

$$\Rightarrow dU_{aus} = dU_1 (g_{m2} r_{DS2} + 1)$$

$$\Rightarrow dU_{aus} = -g_{m1} dU_{ein} \cdot r_{DS1} \cdot (g_{m2} r_{DS2} + 1)$$

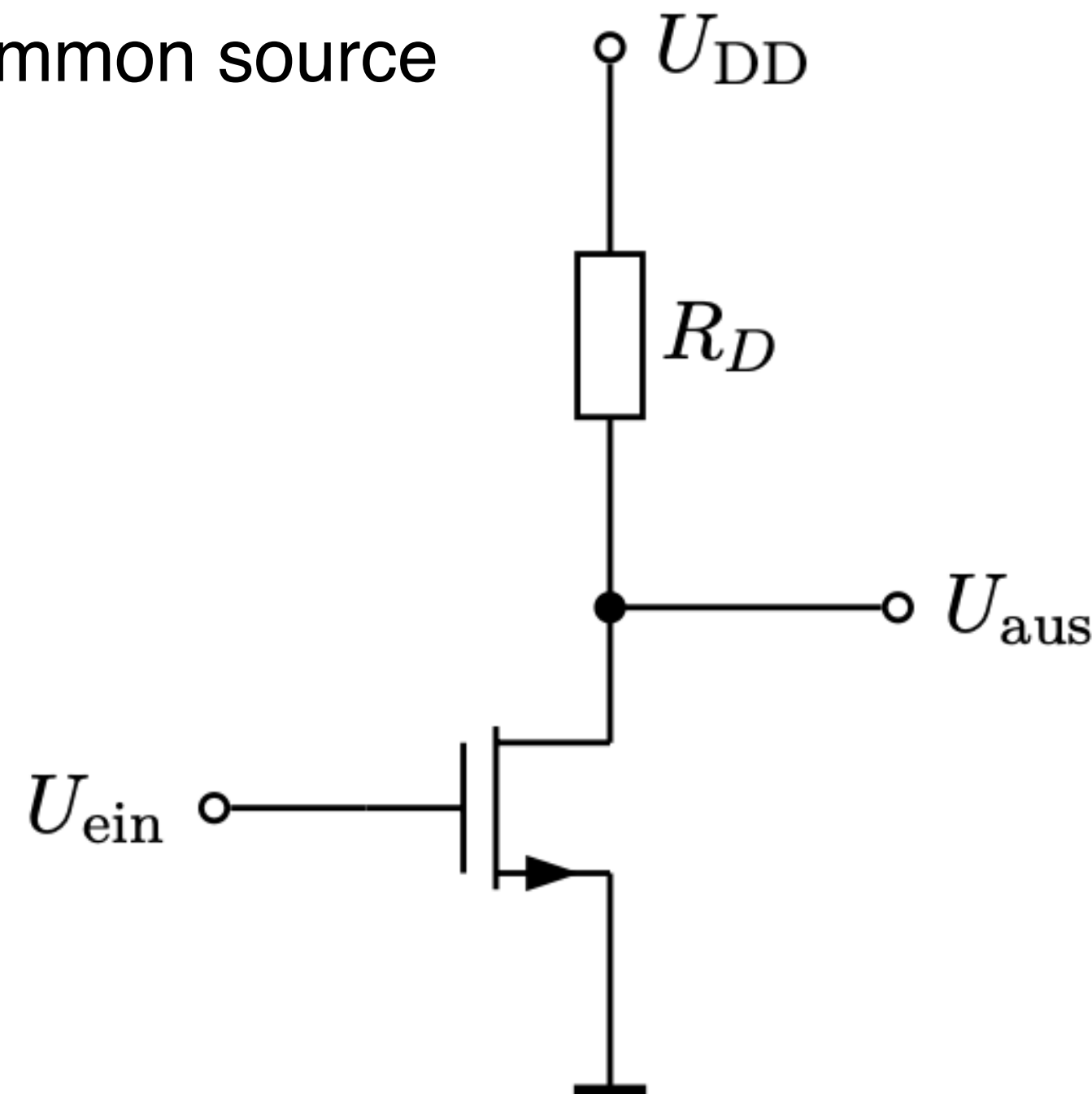
Amplification: $V_U = \frac{dU_{aus}}{dU_{ein}} \approx -g_{m1} r_{DS1} g_{m2} r_{DS2}$

Excursion: CMOS Technology & Transistor Parameters

Consequences for analog Design

- Reminder: Simple amplifier:

NMOS common source amplifier

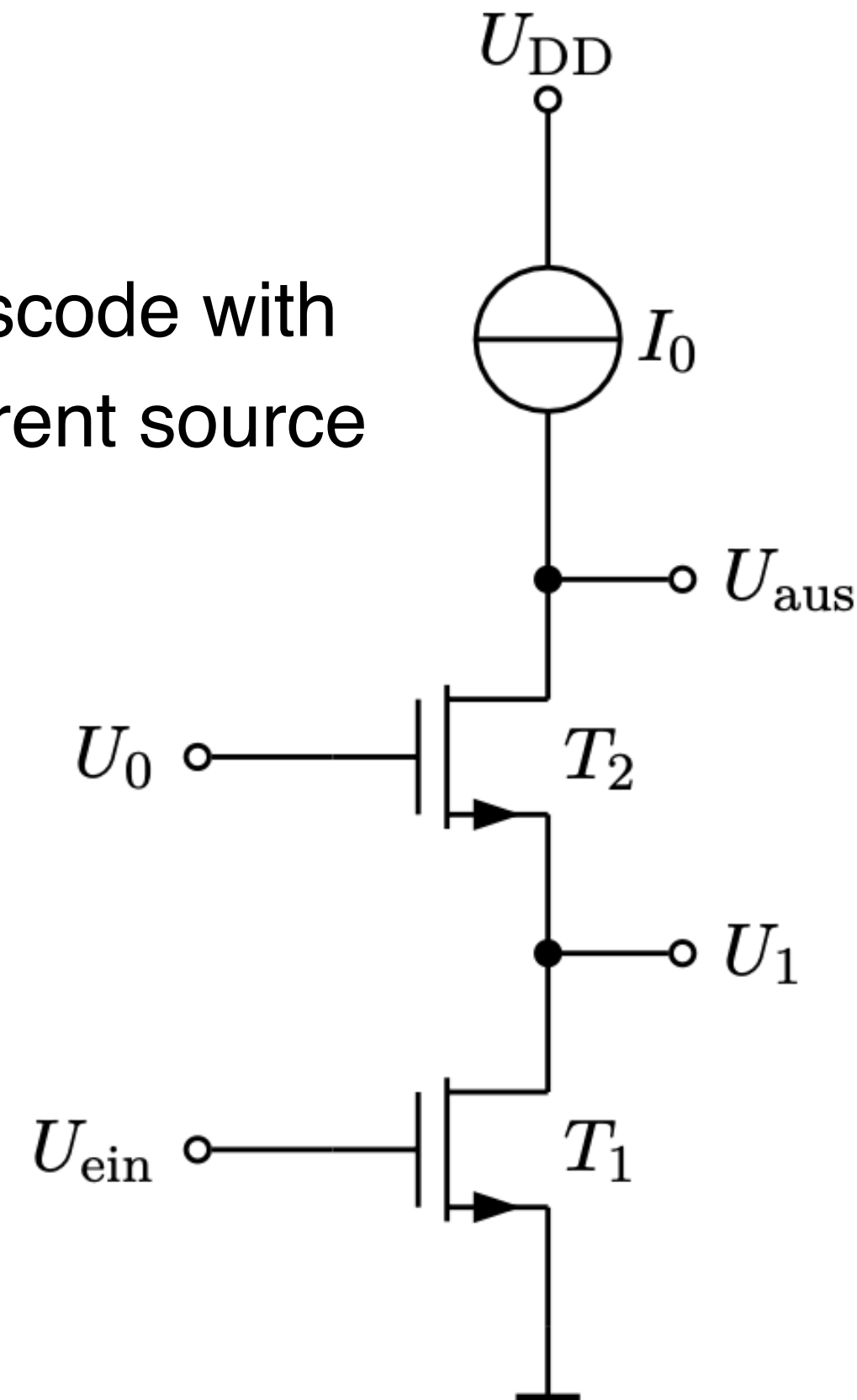


Amplification:

$$V_U = \frac{dU_{ein}}{dU_{aus}}$$

$$V_U \approx -g_m R_D$$

Cascode with current source



Central parameters:

g_m : transconductance

r_{DS} : differential
resistance of transistor

$$V_U \approx -g_{m1} r_{DS1} g_{m2} r_{DS2}$$

Excursion: CMOS Technology & Transistor Parameters

Consequences for analog Design

- Relevant parameters for analog behavior (for example amplification): g_m , r_{DS} ($= 1/g_{DS}$)

Table 1.3 IBM digital CMOS technology characterization, from [26]

Node	nm	250	180	130	90	65
L	nm	180	130	92	63	43
t_{ox}	nm	6.2	4.45	3.12	2.2	1.8
V_{DD}	V	2.5	1.8	1.5	1.2	1
V_{th}	V	0.44	0.43	0.34	0.36	0.24
g_m (peak)	$\mu S/\mu m$	335	500	720	1060	1400
g_{ds}	$\mu S/\mu m$	22	40	65	100	230
g_m/g_{ds}	–	15.2	12.5	11.1	10.6	6.1
f_T	GHz	35	53	94	140	210

from:
Oliveira, Goes: “Parametric Analog Signal Amplification Applied to Nanoscale CMOS Technologies”, Springer, DOI 10.1007/978-1-4614-1671-5

g_m , r_{DS} (and with that the amplification) degrades for smaller transistors.

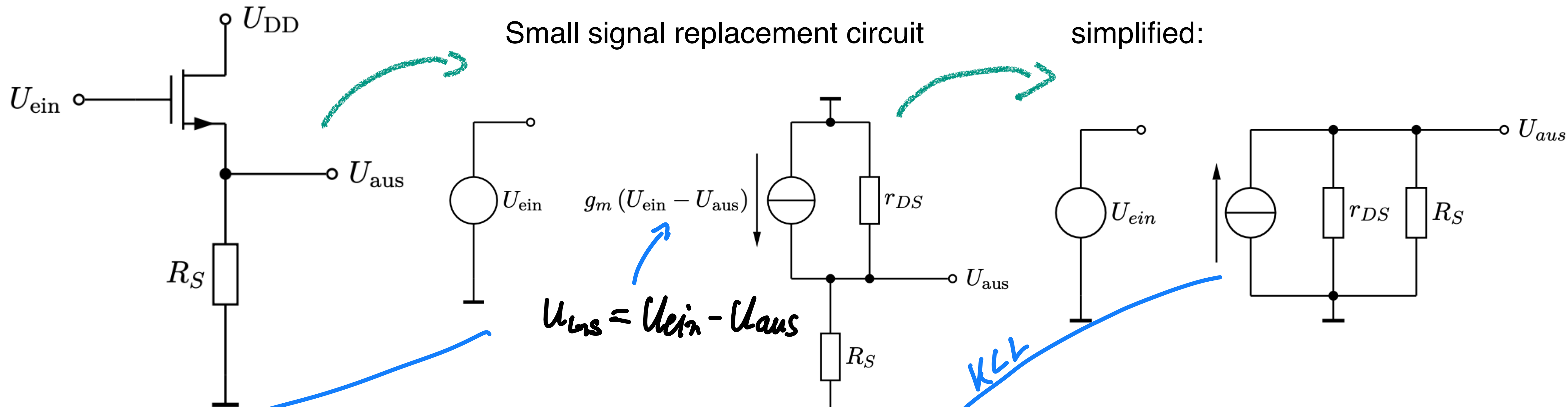
(Re-)optimization, or even specific redesign of a circuit for a new technology required!

In a short conclusion, technology scaling tends to achieve a higher g_{ds} in saturation which degrades the gain but, at the same time, due to limited voltage range, the g_{ds} in linear region tends to be lower, degrading the ON resistance of the switch.

relative to width w
 $\Rightarrow g_m \cdot r_{DS}$
 $\hookrightarrow$ amplification for cascode etc.

Source Follower / Common Drain

The FET Equivalent of the common Collector



$$I_{DS} = g_m dU_{GS} = g_m d(U_{\text{ein}} - U_{\text{aus}})$$

$$= \frac{dU_{\text{aus}}}{R_S \parallel r_{DS}} = \frac{dU_{\text{aus}}}{R_S'} \quad (R_S' = R_S \parallel r_{DS})$$

$$dU_{\text{aus}} (1 + g_m R_S') = dU_{\text{ein}} g_m R_S'$$

$$V_u = \frac{dU_{\text{aus}}}{dU_{\text{ein}}} = \frac{g_m R_S'}{1 + g_m R_S'} < 1$$

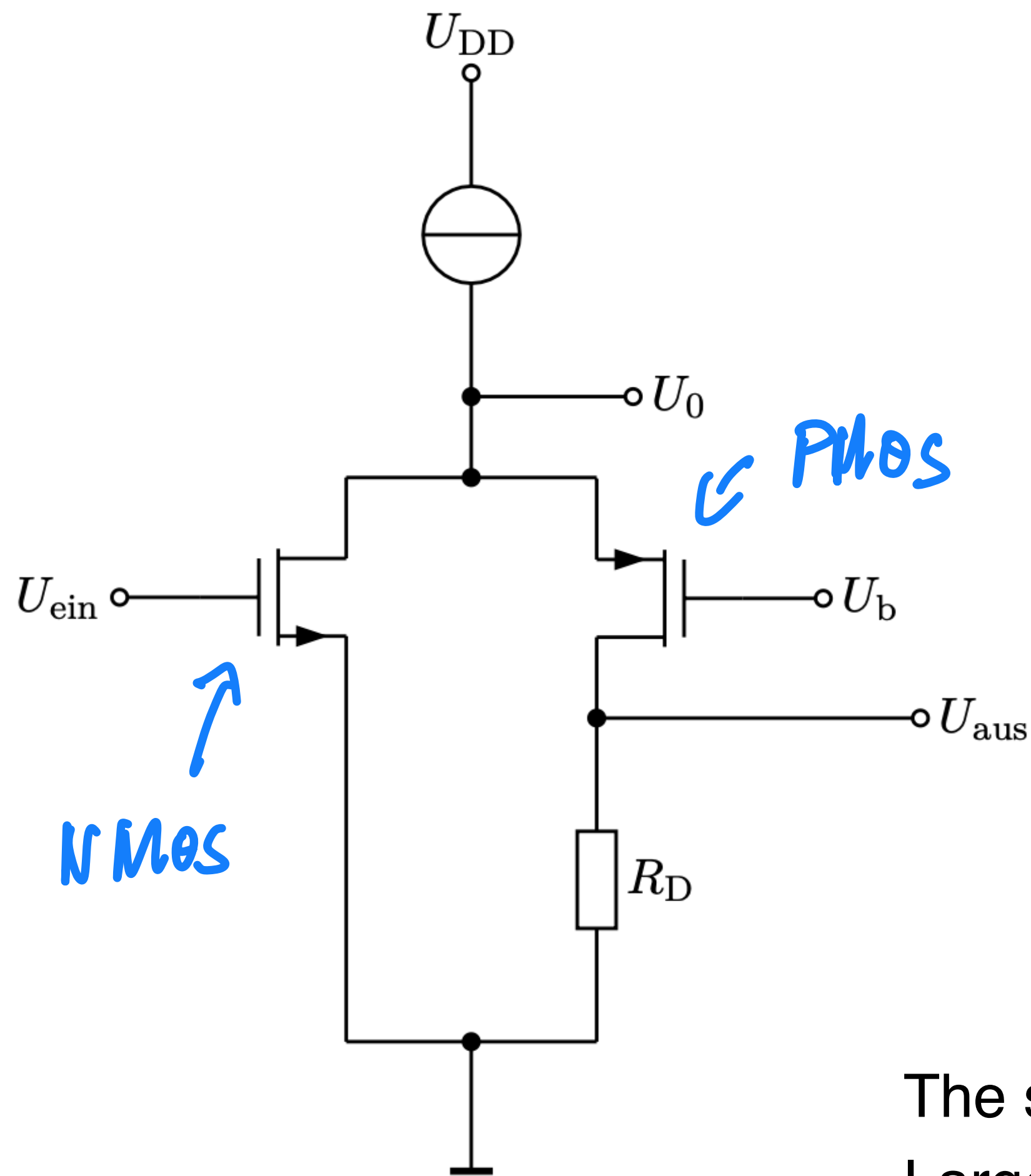
in addition: $R_{\text{in}} \rightarrow \infty$

$$R_{\text{aus}} = \frac{dU_{\text{aus}}}{dI_{\text{aus}}} = \frac{1}{g_m} \parallel R_S'$$

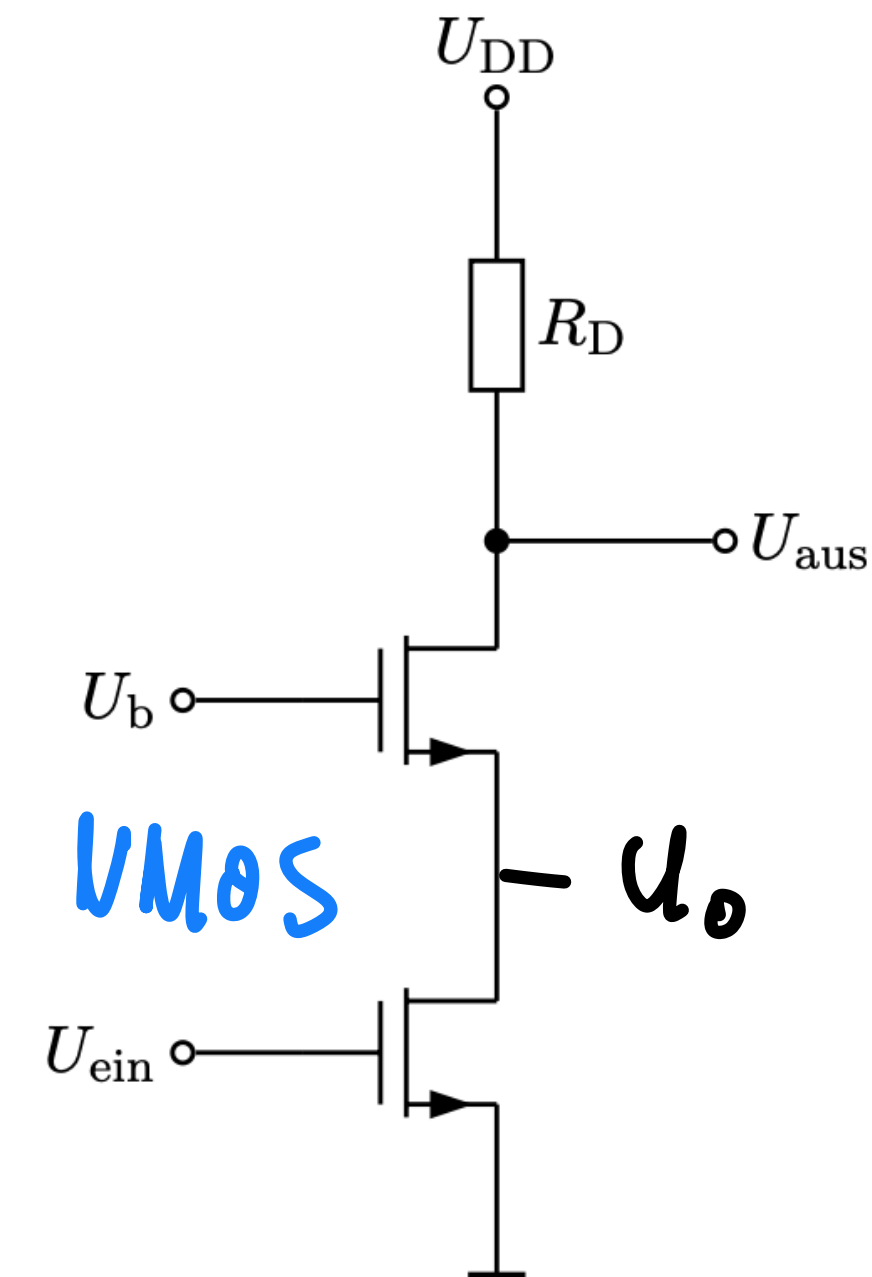
FYI: Folded Cascode

A Variation of the “regular” Cascode

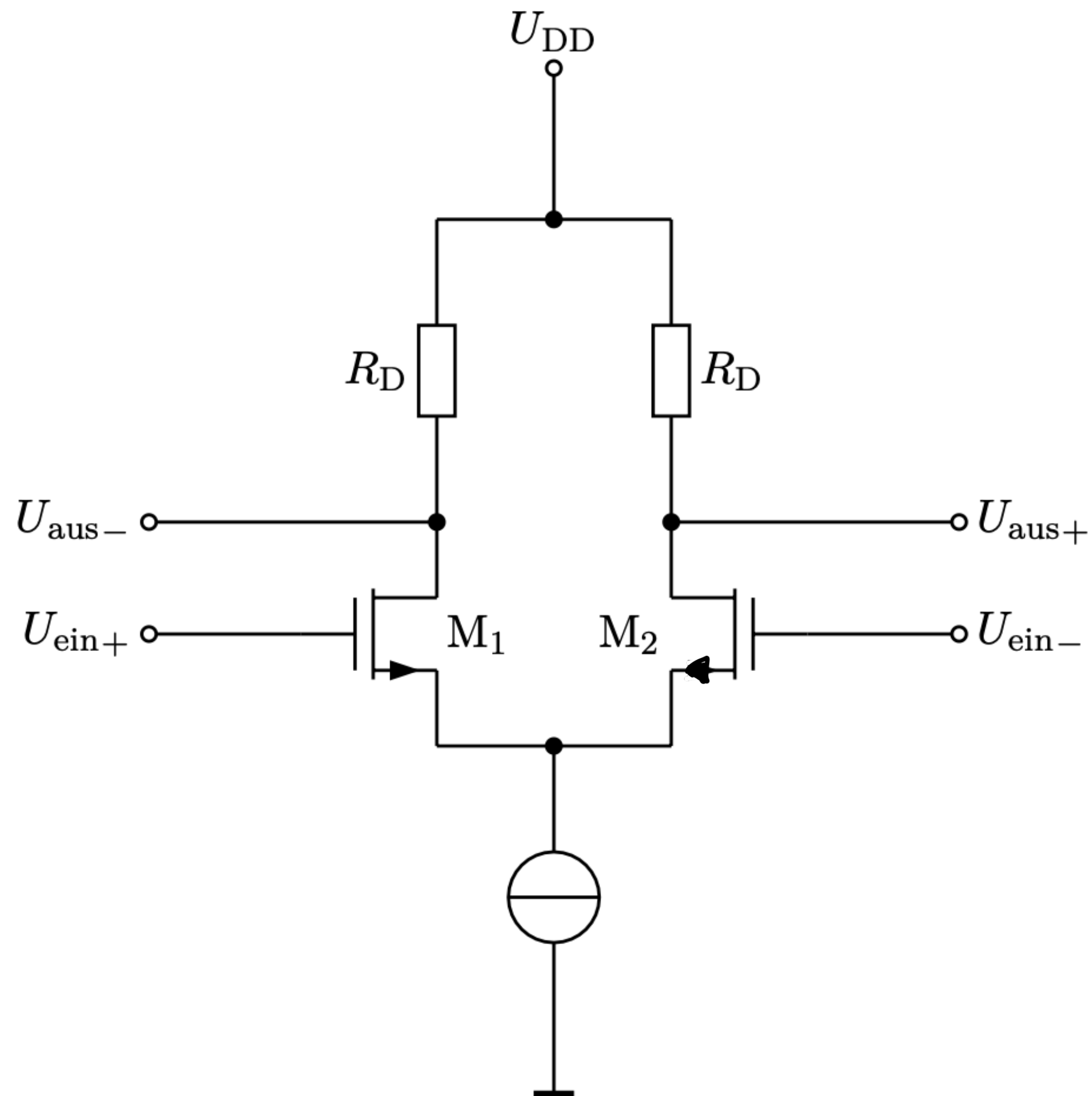
- An alternative implementation of the cascode: Current split across two branches (similar to differential amplifier)



compare to: “regular” cascode



The strength of this circuit:
Larger dynamic range in output voltage!



- The basic implementation

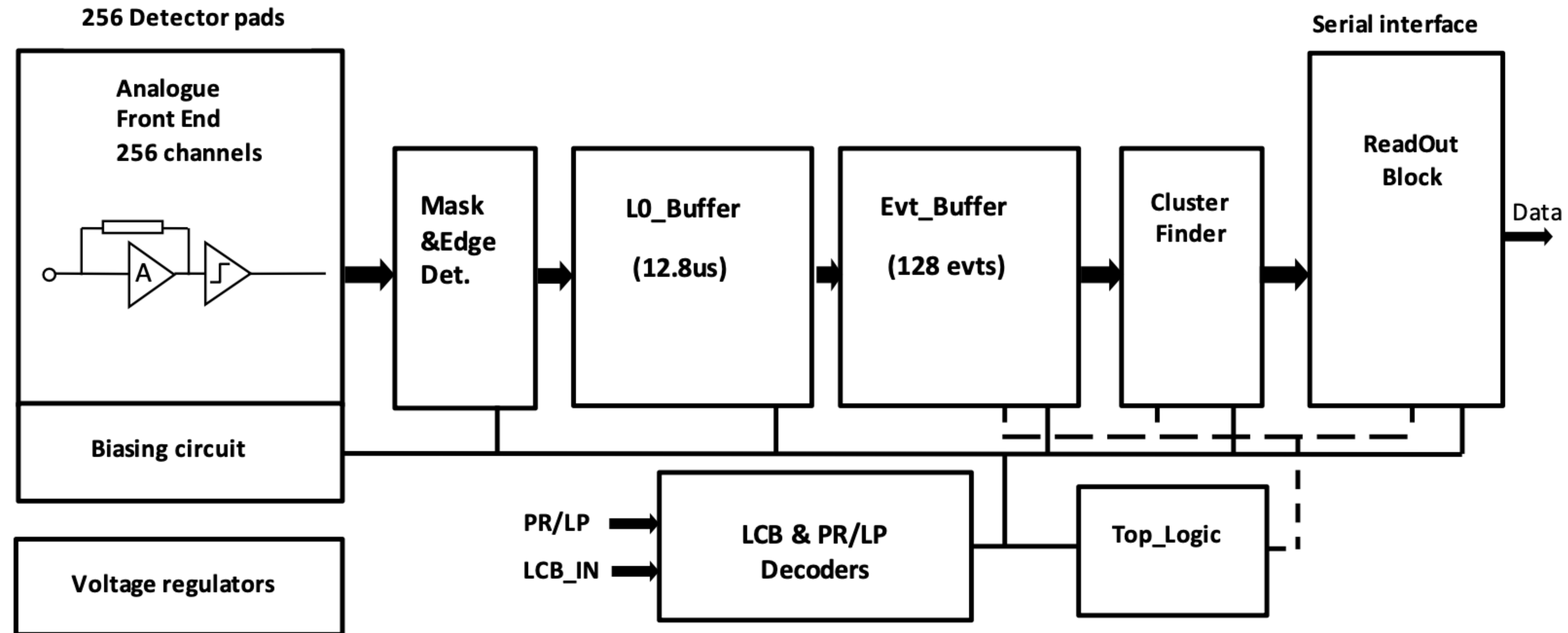
$$V_U = \frac{dU_{\text{aus}}}{dU_{\text{ein}}} = \frac{dU_{\text{aus}+} - dU_{\text{aus}-}}{dU_{\text{ein}+} - dU_{\text{ein}-}} = -g_m R_D$$

... and a range of further improvements, the same as for the BJT

As an Example: A real Circuit

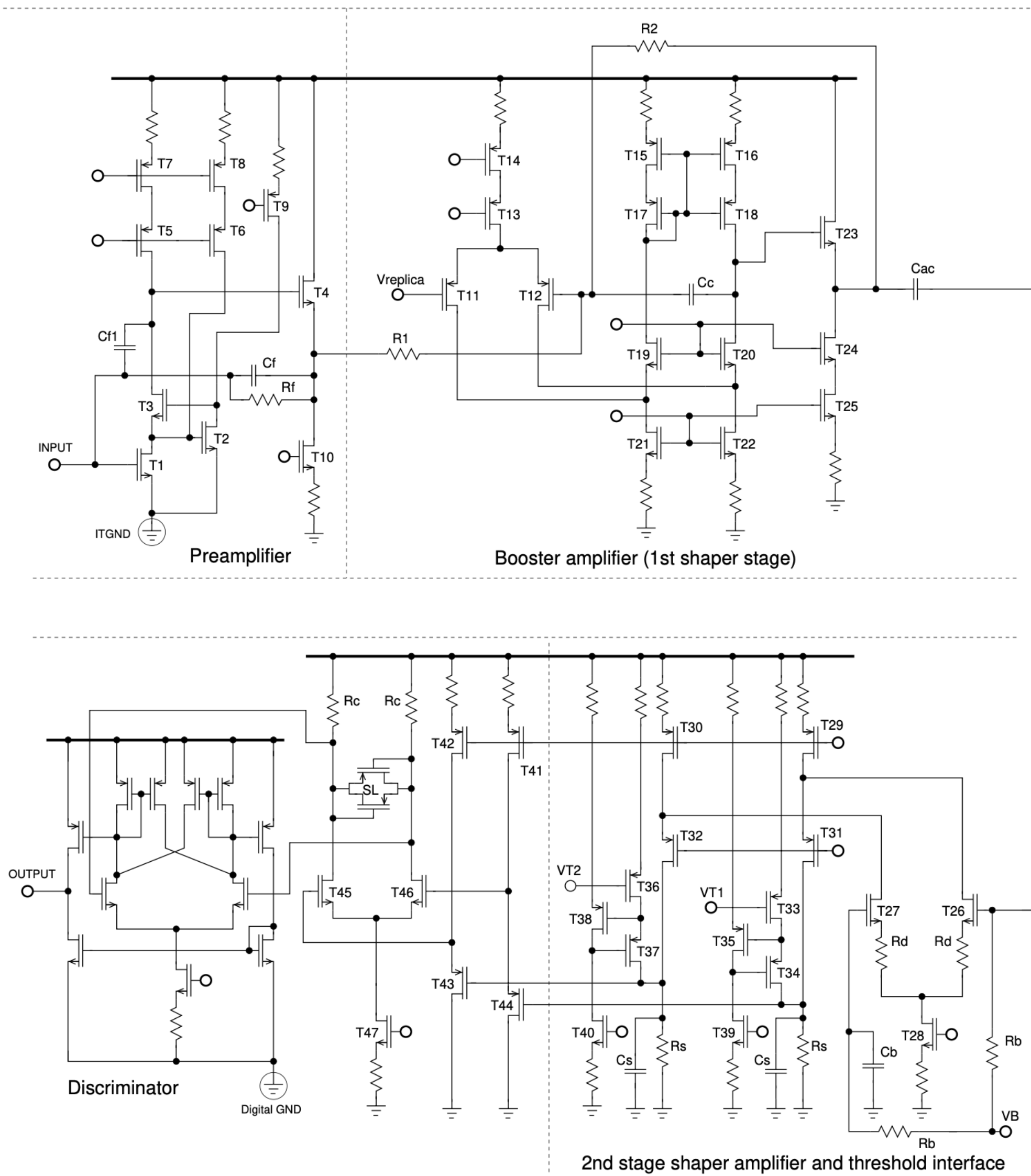
ATLAS Phase II Silicon Strip Detector (ITk Strips): Front-end ASIC ABCStar

- A complex ASIC with analog and digital parts



As an Example: A real Circuit

ATLAS Phase II Silicon Strip Detector (ITk Strips): Front-end ASIC ABCStar



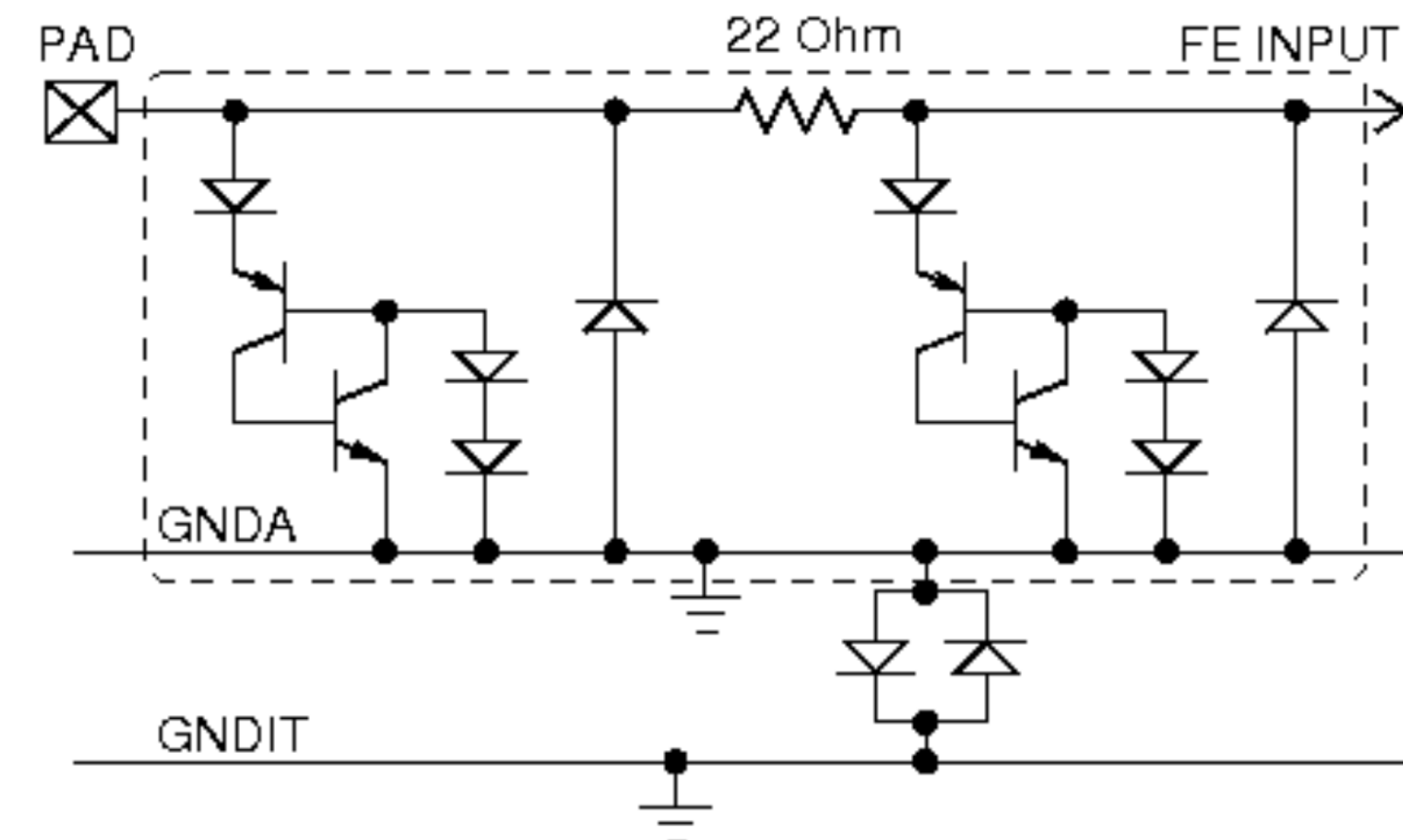
The analog front-end: 256 copies in the chip

Finally: Binary readout (strip hit or not)

But: Thresholds etc. require an analog processing of the signals.

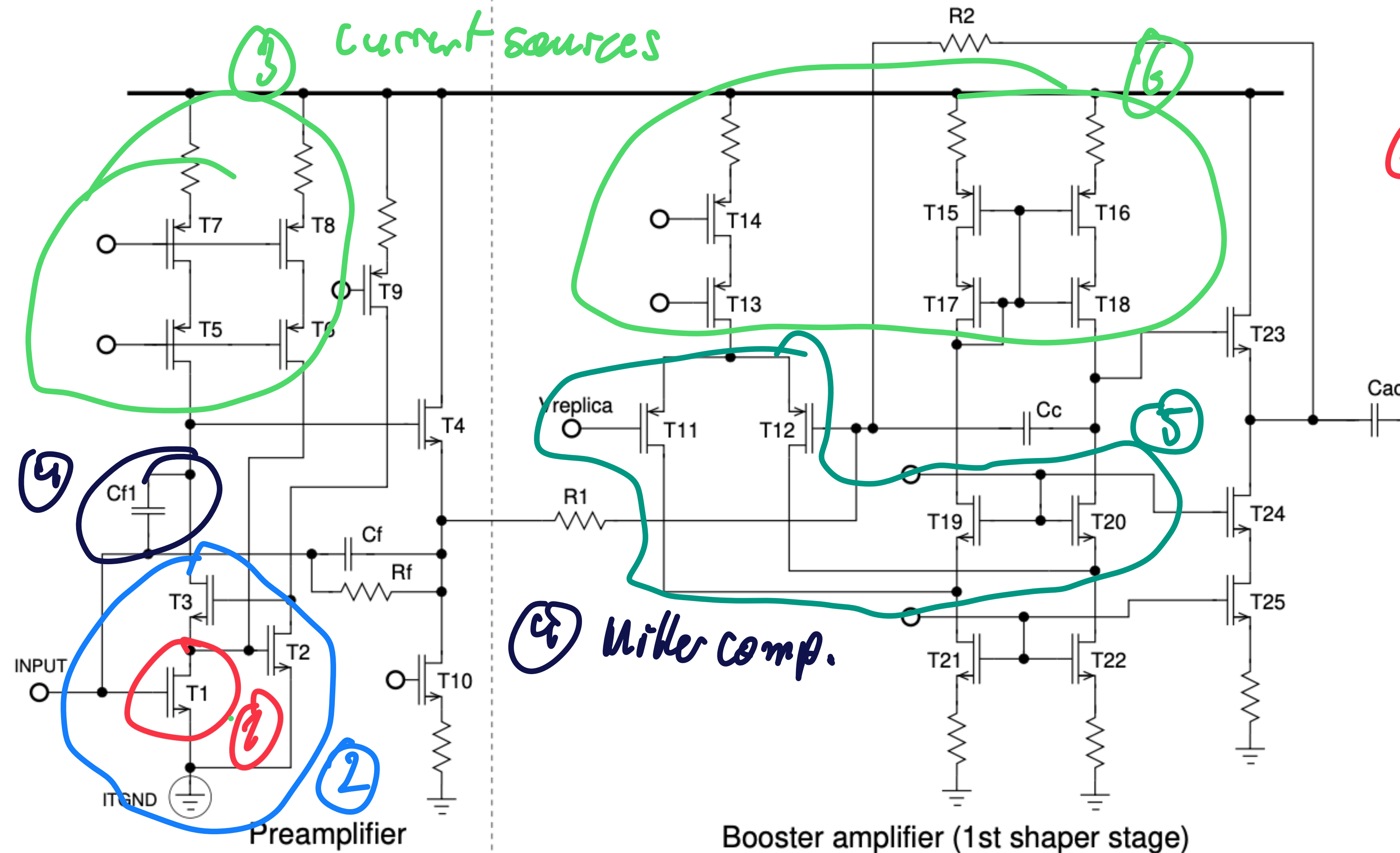
4-step circuit as analog front-end

In addition: protection circuit on input



As an Example: A real Circuit

ATLAS Phase II Silicon Strip Detector (ITk Strips): Front-end ASIC ABCStar



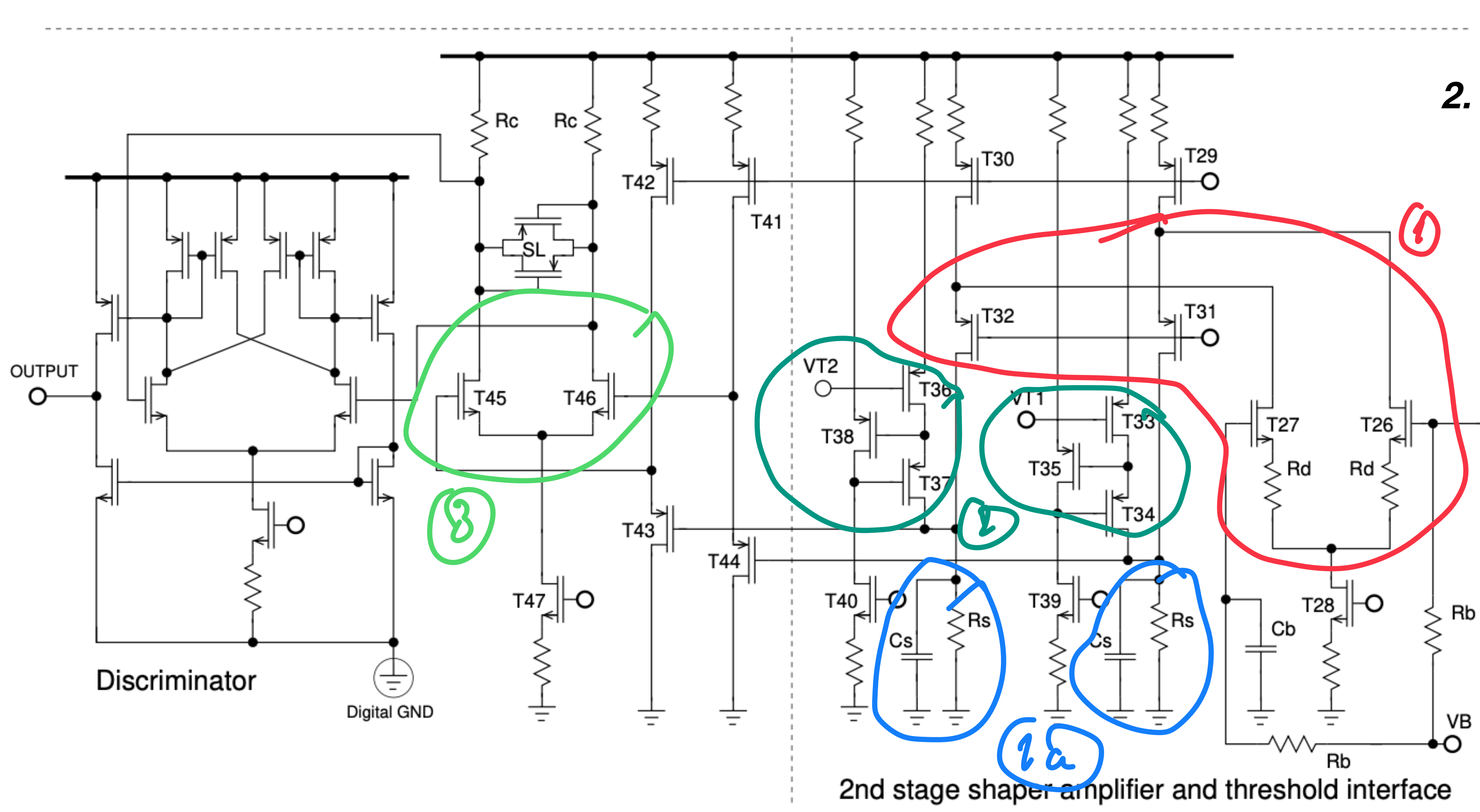
1. Part: Pre-amp; Booster

- ① Input NMOS
Gate: $316\mu\text{m} \times 300\text{nm}$
Input-C 600fF , matched
to 60fF strip C (5cm)
- ② Regulated
Cascode
- ③ diff. input
folded cascode
- ④ current sources/
mirrors

As an Example: A real Circuit

ATLAS Phase II Silicon Strip Detector (ITk Strips): Front-end ASIC ABCStar

2. Part: Shaper, Discriminator



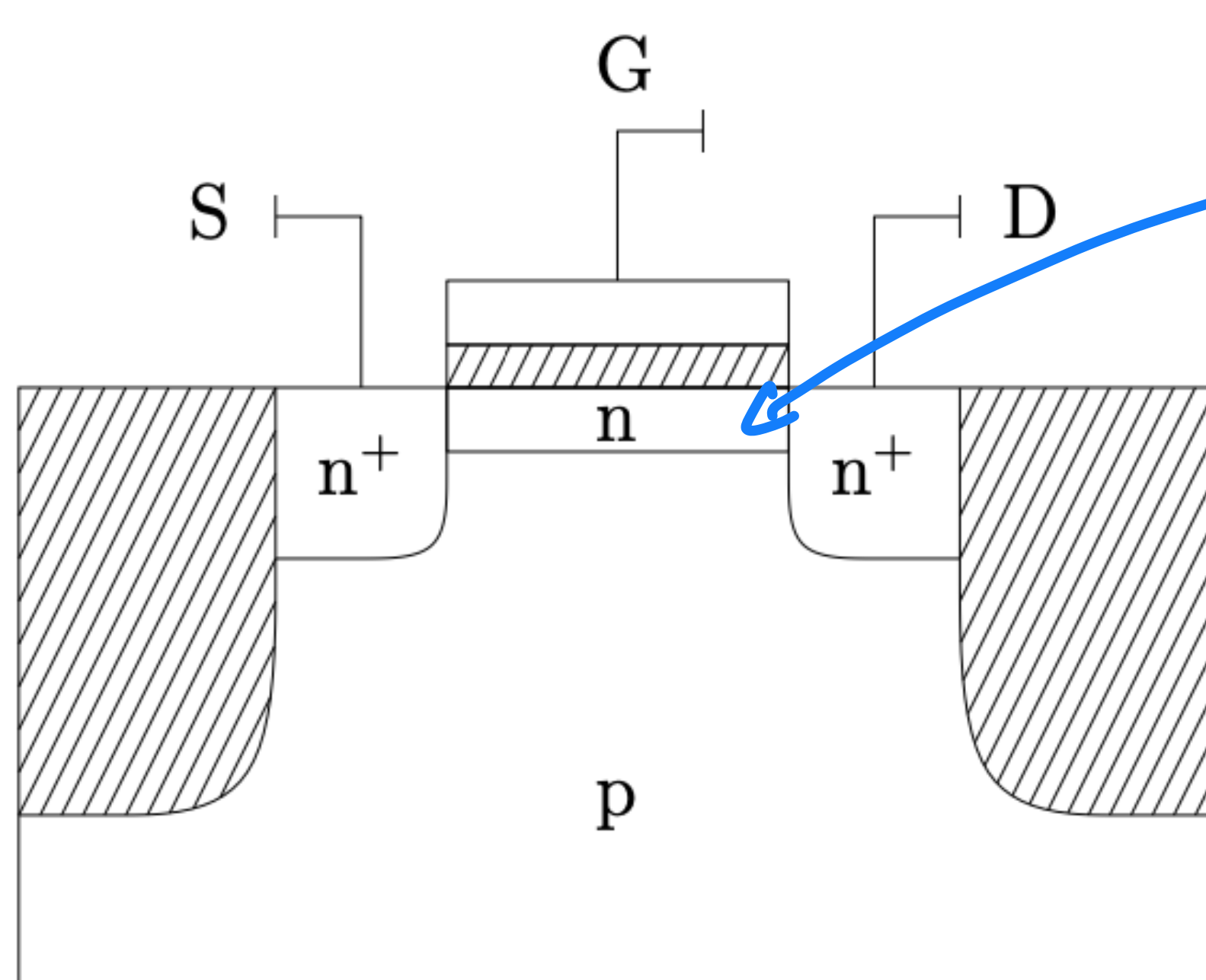
- ① Diff. folded cascode
- ② integration of signal
- ③ high-impedance current sources VT_1, VT_2 input to set threshold, ch-by-ch. corrections
- ④ differential amplifier: input to discriminator

Other Transistor Types

In: Chapter 7: Field Effect Transistors

Depletion-mode MOSFETs

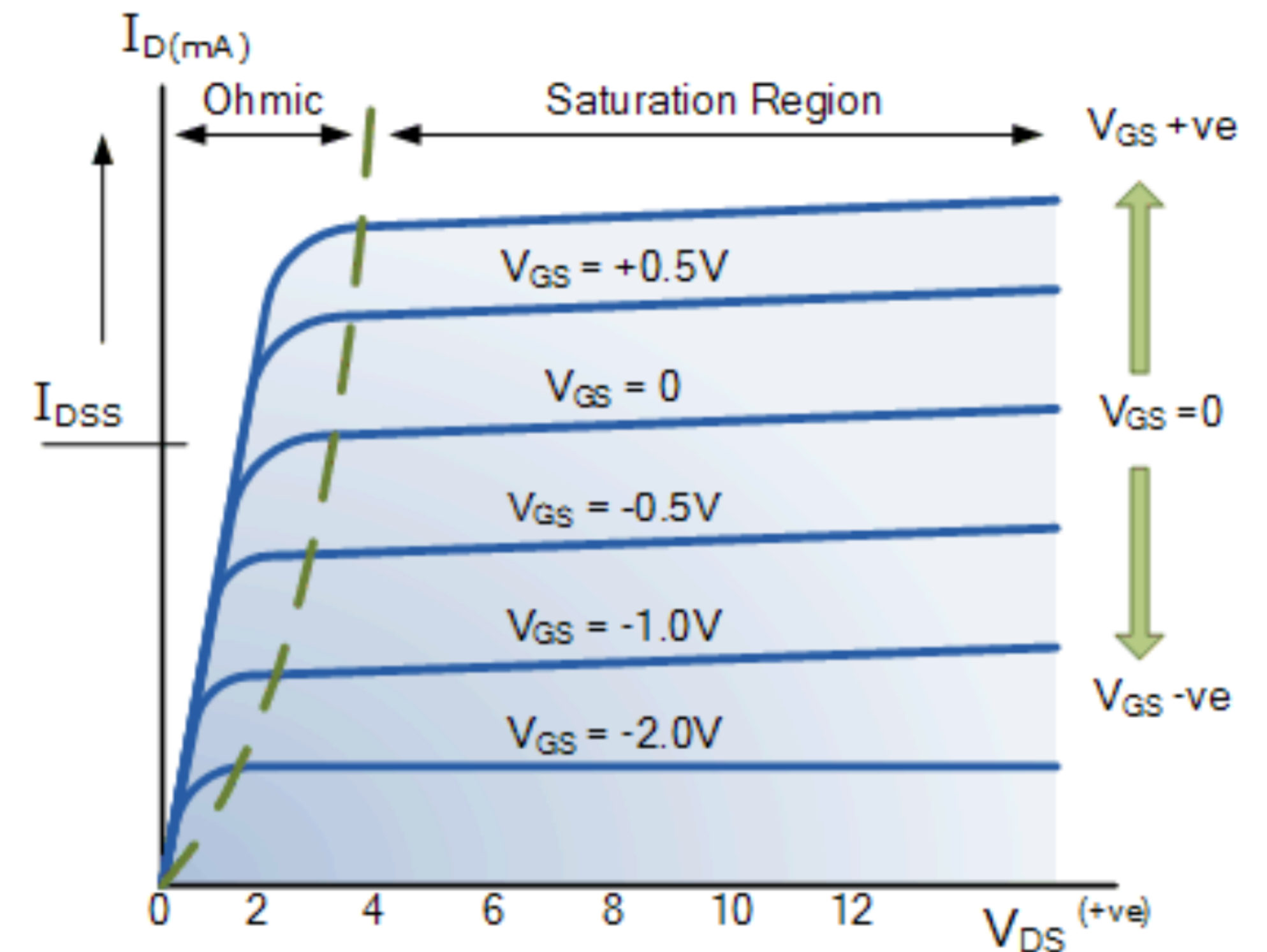
Selbstleitende MOSFETs



Conductive channel
(due to n doping)

- Conductive for $U_{GS} = 0$: negative threshold voltage
- Non-conductive only for significantly negative U_{GS}

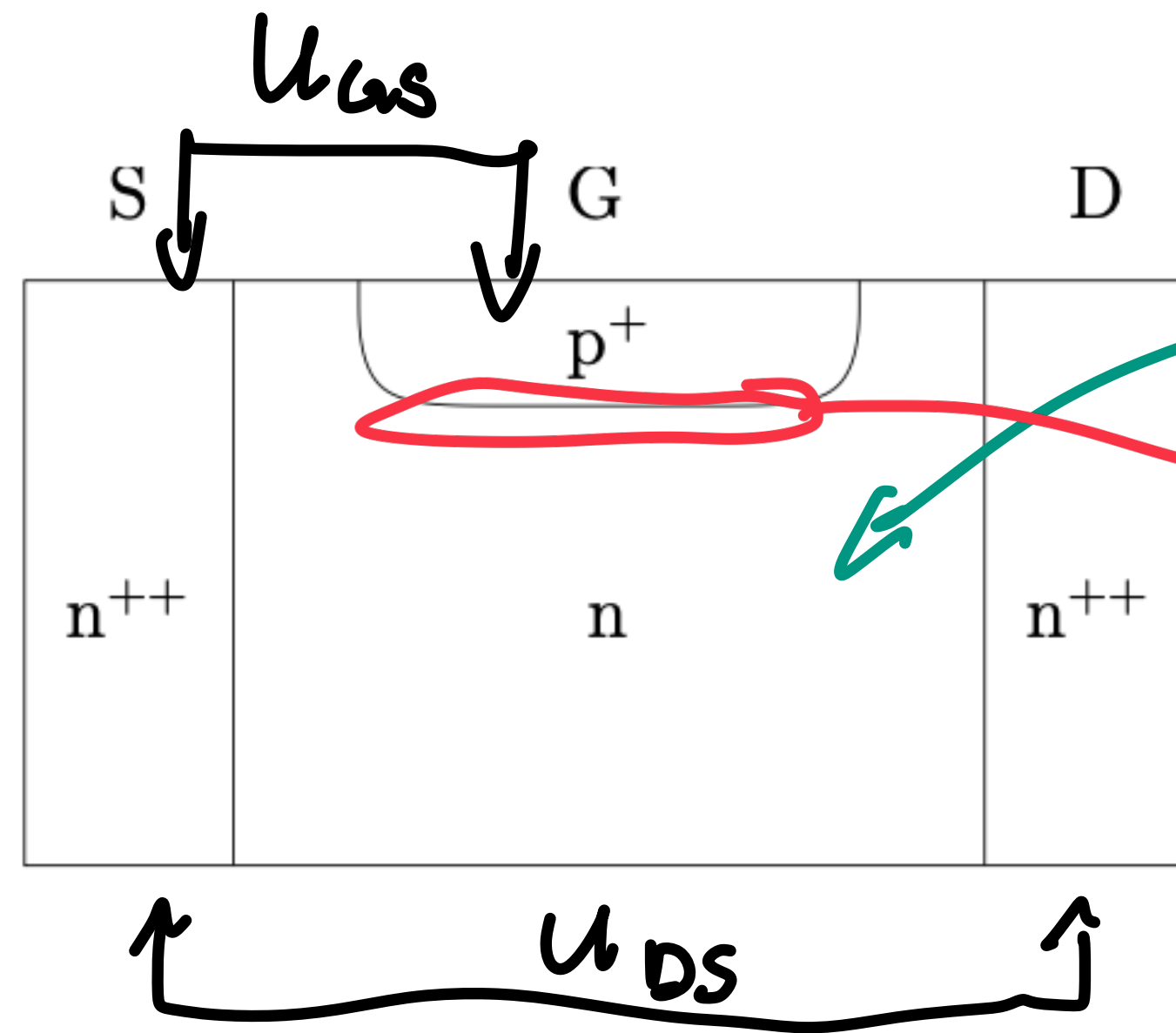
- Two types of MOSFETs:
 - Enhancement-mode (Anreicherungs-Modus)
The most common variant - considered up to now
 - Depletion-mode (Verarmungs-Modus)



from Electronics Tutorials

JFET: Junction FET

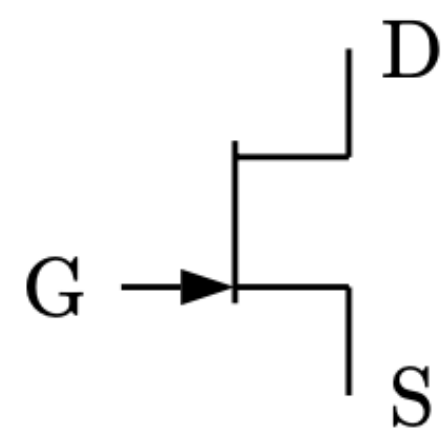
Sperrschicht-FET



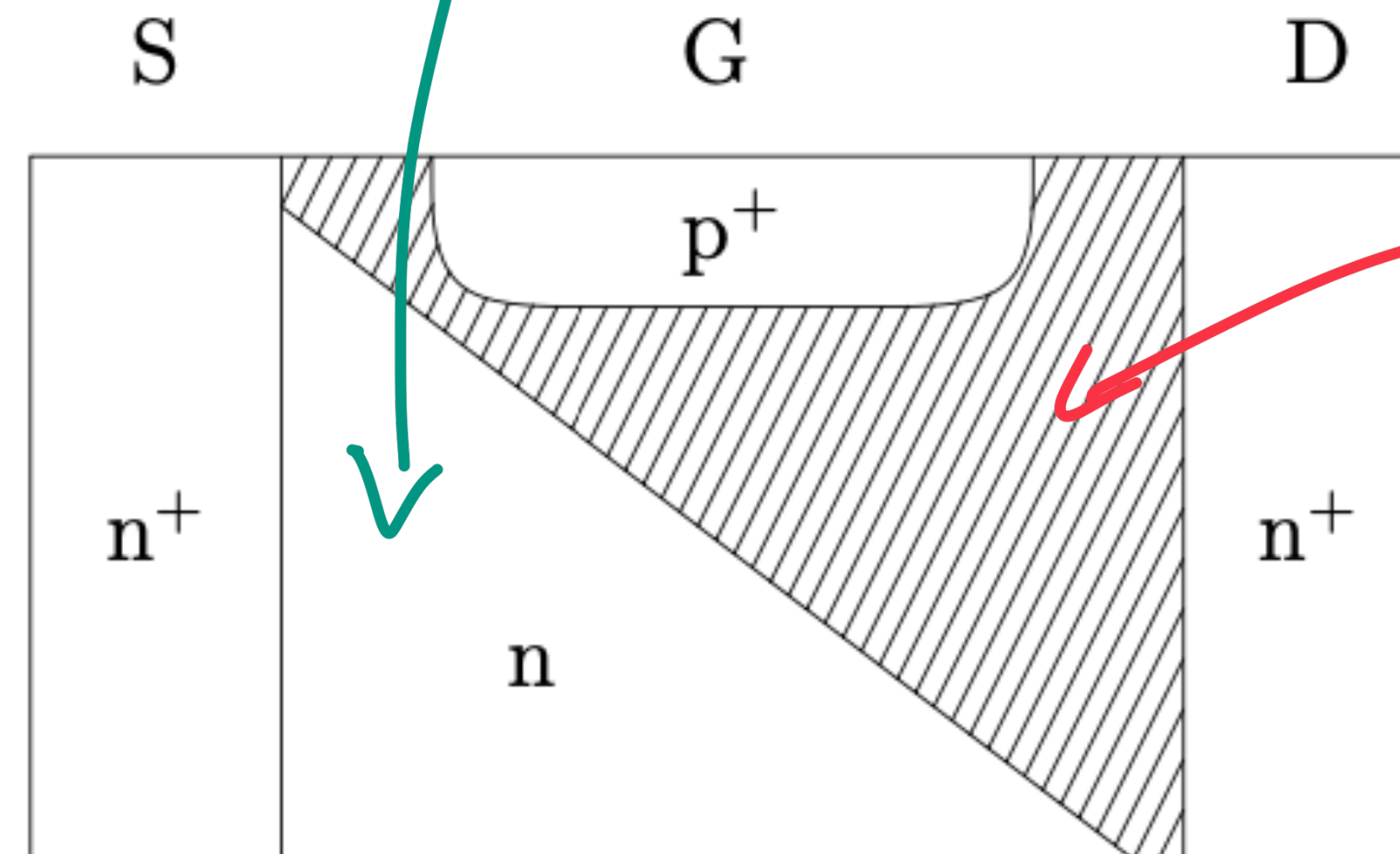
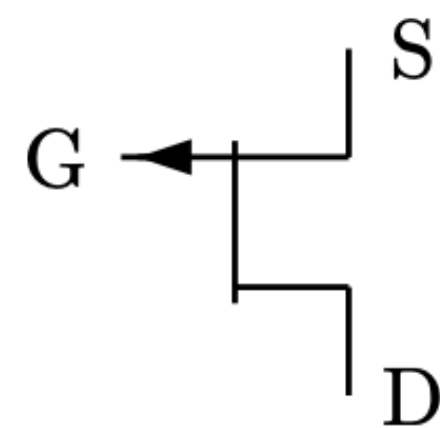
- n-conductive channel between source and drain at $U_{GS} = 0$
- Negative U_{GS} pinches off the channel:
Reduction of I_{GS}
- $U_{GS} \leq 0$, $U_{DS} > 0$, results in reverse-bias on pn-junction: (Almost) no current from G to D

As two types:

n-channel

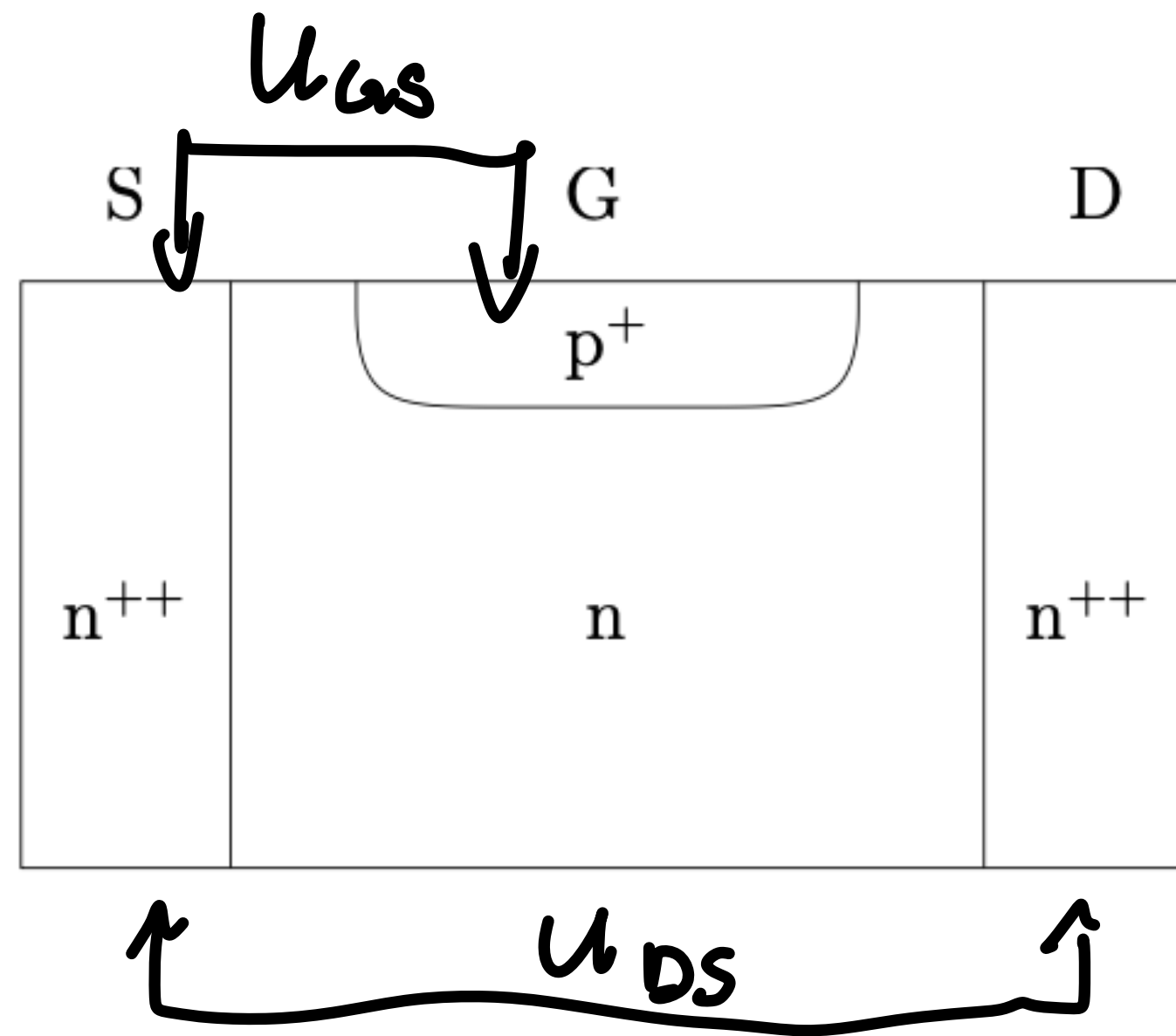


p-channel



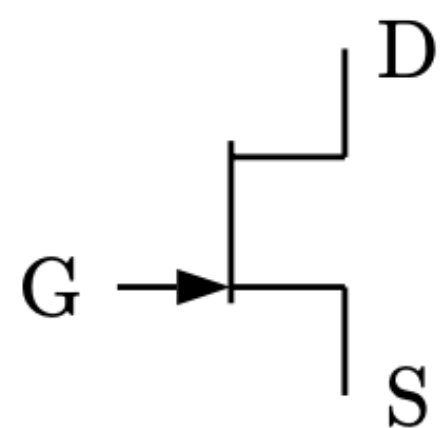
JFET: Junction FET

Sperrschicht-FET

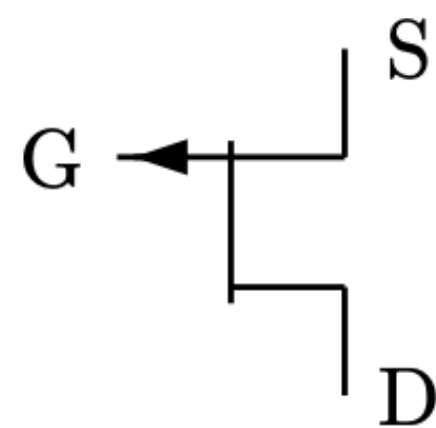


As two types:

n-channel



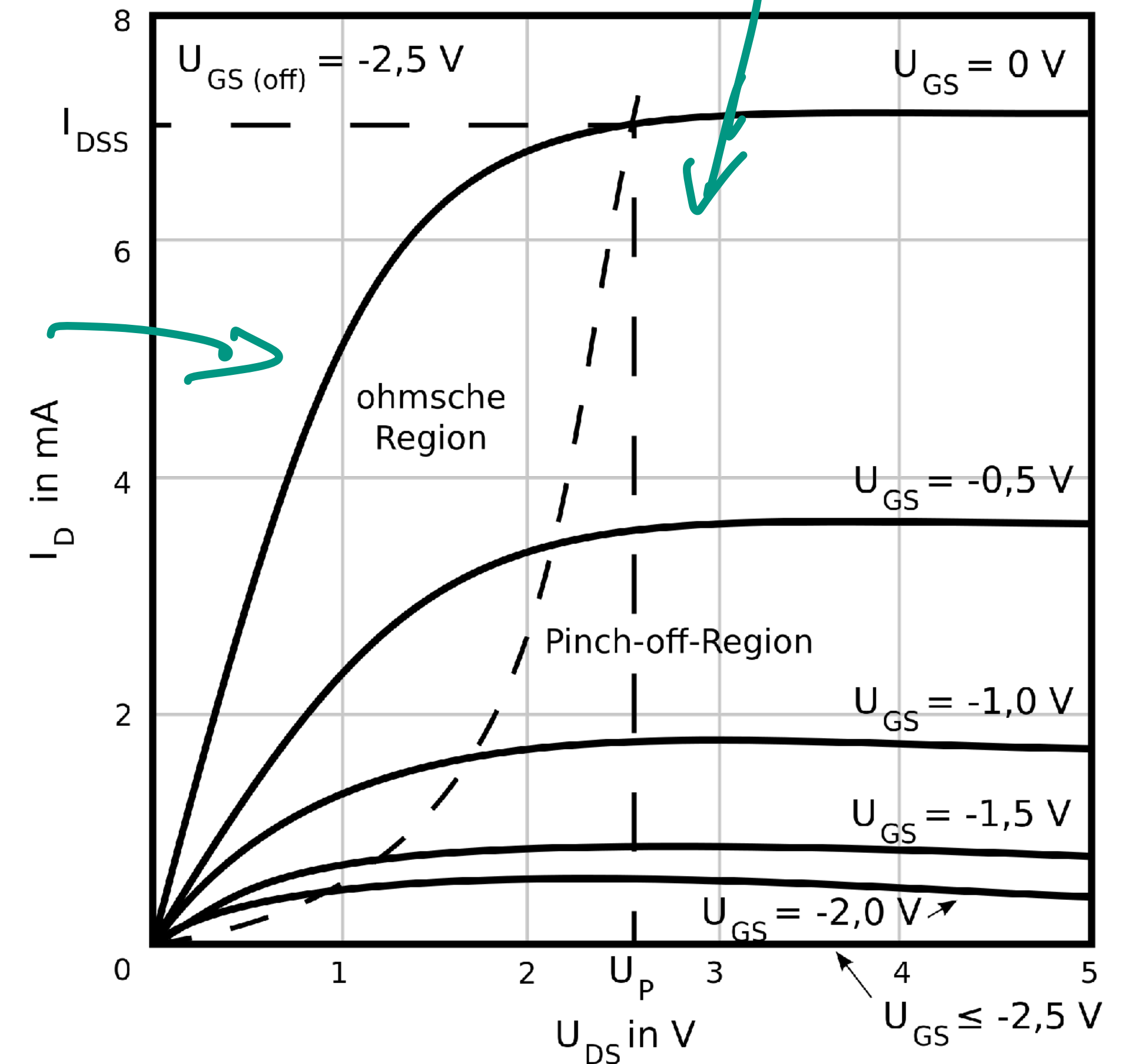
p-channel



- Typical IV curve:

linear / ohmic region

saturation region / pinch-off



Typisches Ausgangskennlinienfeld eines n-Kanal-JFET

Next Lectures:

Analog 14 - Chapter 08 - Thursday, February 8, 2024

Analog 15 - Chapter 08 - Tuesday, February 13, 2024

Time Plan for Next Lectures

A few Changes coming up!

Calender Week	Tuesday	Thursday
45	07.11. Analog	09.11. Digital
46	14.11. Analog	16.11. Digital
47	21.11. Digital	23.11. Analog
48	28.11. Digital	30.11. Digital
49	05.12. Digital	07.12. Analog
50	12.12. Digital	14.12. Analog
51	19.12. Analog	21.12. Digital
2	09.01. Analog	11.01. Digital
3	16.01. Digital	18.01. Digital
4	23.01. Analog	25.01. Digital
5	30.01. Analog	01.02. Digital
6	06.02. Analog	08.02. Analog
7	13.02. Analog	15.02. None

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